Design of an Energy-Efficient D Flip-Flop Utilizing Graphene Nano-Ribbon Field Effect Transistors (GNRFET) in 22nm Technology with Integrated Sleep Mode Functionality

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Abstract- It has immense importance in both applications, storage and circuitry; however, its developments advance PDPs power delay characteristics, as well. Hitherto, even this area of static as well as dynamic D flip-flops varied extensively within literature, but effectiveness for use in energy and consumption of power has not so far been achieved. This thesis proposes an attempt to modify the existing D Flip-Flop using the Graphene Nano Ribbon Field Effect Transistor (GNRFET) in the 22nm technology channel. In this modification, it aims to save energy by incorporating a Sleep Mode concept, preventing energy dissipation from taking place wastefully. From the results of simulations run on the HSPIce program for the proposed circuit, the performance in terms of mean power, time delay, and energy dissipation is superior. The voltage source dissipation provided by the GNRFET designs is almost indistinguishable from and clearly better than that given by bulk CMOS MOSFET equivalents. This therefore goes to show that GNRFET is a viable substitute to channel length technologies within the 22nm category.

Keywords: D Flip-Flop, GNRFET, PDP, HSPICE

Introduction

The D flip-flop is an important memory cell that is used in digital circuits and is an important component overall. This is due to the fact that it can switch between two different states at will. It is also often employed in huge flip-flop arrays as well as in digital integrated circuits since it has such a wide variety of uses. This is because it has such a broad range of applications. The relevance of designing new D flip-flops and improving existing ones has steadily been on the rise during the last few years due to the ongoing pace of technological innovation as well as the increasing complexity of digital circuits. This is a reaction to both factors. This is the case because both of these causes are contributing towards the complexity that is being seen in digital circuits. This study proposes to improve the performance of D flip-flops by using Graphene Nano Ribbon Field Effect Transistors (GNRFET) in the 22nm technology channel and by creating a Sleep Mode idea in order to lower the amount of energy that is lost when the device is running. The purpose of this research is to reduce the amount of energy that is lost when the device is functioning. These two are being looked at to the light as a solution to reduce the waste of electricity that is wasted.

Despite the fact that the present body of study has suggested a number of unique static and dynamic D flip-flops, the most effective utilization of energy and power has not yet been accomplished. Within the confines of this thesis, we attempt to address the problem by introducing further enhancements to the power-delay product with the help of the specific operating modes enabled by the GNRFETs while reducing the overall number of transistors. In that process, we hope to find a way to be able to find a solution to this problem. The motivation behind this specific area of research was the idea that high-performance TSPC D flip-flops may be constructed making use of GNRFET technology. If successful, the devices produced would have a power-delay significantly reduced, and their energy efficiency enhanced to a great degree, making them a fantastic option for high-speed digital integrated circuits.

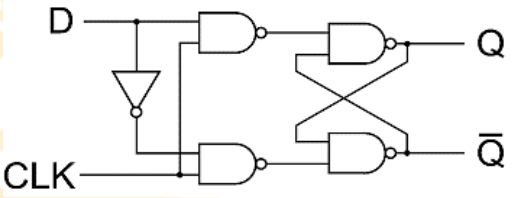

Figure 1: DFF

The primary objectives of this study are to develop an accurate and efficient system using GNRFET in dynamic DFF, to design a low power circuit with Sleep Mode to prevent short circuit power consumption, to create a high-speed D flip-flop using GNRFET in 22nm technology for a variety of applications, and to design an energy-efficient TSPC D flip-flop using GNRFET. All these goals will be achieved using the device GNRFET. Other goals are the development of a low-power circuit with a sleep mode, which will avoid the waste of power by short circuits. The attainment of these goals will be very

effective with the development and implementation of a high-speed D flip-flop.

The primary aim of this research will be to design and implement a better D flip-flop utilizing the 22nm technology channel that incorporates GNRFET. This will be the end outcome of the study. It will form the main concern of the study. To illustrate the benefits of the design that has been proposed, it will be compared with alternative ways in terms of the amount of energy it consumes, the amount of time it takes, and the amount of energy it wastes. The results of this study will lead to the creation of D flip-flops that not only have a high degree of performance but are also efficient in terms of how they utilize the energy that they use. The use of these flip-flops is going to be necessary for the operation of digital circuits. This will enable designing more complex devices that are also sensitive to the amount of power they consume. This is particularly important in the portable electronics area, where a low level of power consumption is very critical. This will enable the development of more complex devices that are also conscious of the amount of power they consume.

In a nutshell, the goal of this research was to improve the performance of D flip-flops that employ GNRFET in the 22nm technology channel while also improving their energy efficiency. This will be achieved through the implementation of a technique referred to as Sleep Mode, whose objectives are to save energy and minimize the unnecessary or excessive dissipation. The findings of this research will have a significant impact on the growth of the portable electronics sector, information dissemination on devices that have a low impact on the environment, and new digital circuits for more complex computing.

Implementation

This research employed the parameters of the GNRFET technology in all circuits made; Table 1 summarizes all the parameters. The parameters illustrated here are utilized in coding the circuits within Synopsys HSPICE; however, HSPICE does not include a schematic creator. All circuits done on paper in node form before entry into HSPICE for encoding.

Table 1: GNRFET Technical Parameters

Parameter	Description	Value
nRib	The number of GNRs in the device.	3
n	The number of dimer lines in the GNR lattice	6
L	Physical channel length.	22n
Tox	Oxide Thickness between channel and substrate/bottom gate	0.95n
sp	The spacing between the edges of two adjacent GNRs within the same device	1n
dop	Source and Drain reservoirs doping fraction	0.001

The circuits for the research study, including the TSPC-based D flip-flop and the modified TSPC-based D flip-flop, are implemented using GNRFET technology, as shown in Figures 2 and 3.

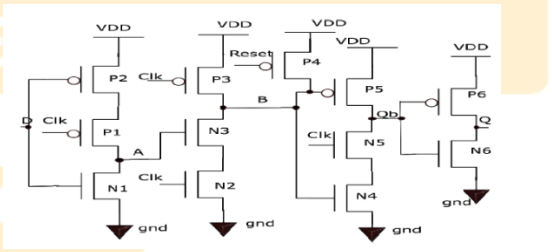

Figure 2: DFF

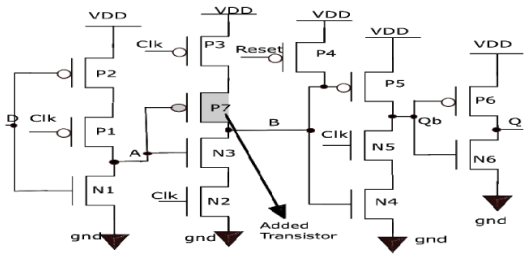

Figure 3: MTSPC based DFF

Figures 4 and 5 show the TSPC-based D flip-flop and modified TSPC-based D flip-flop implemented using GNRFET 22nm technology in LTSPICE. Figure 6 shows the proposed sleep mode for the modified TSPC-based D flip-flop circuit.

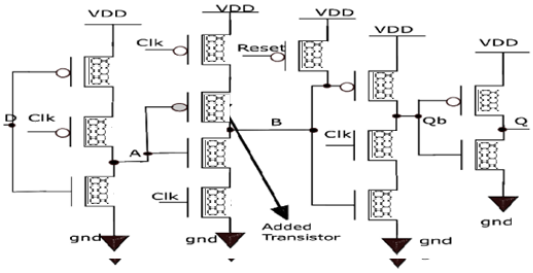

Figure 4: TSPC DFF GNRFET

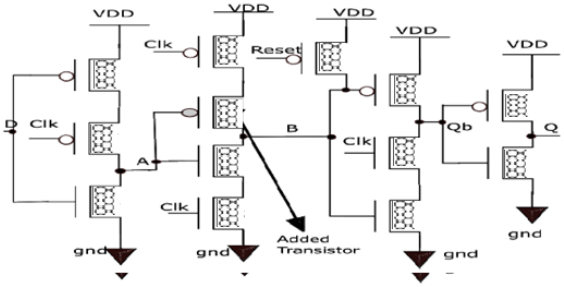

Figure 5: MTSPC DFF GNRFET

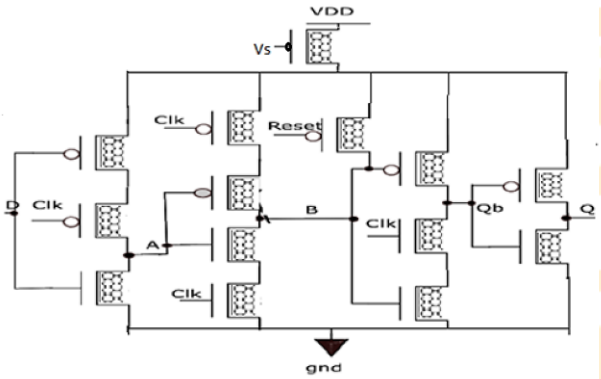

Figure 6: MTSPC Sleep Mode DFF GNRFET 22nm

Results

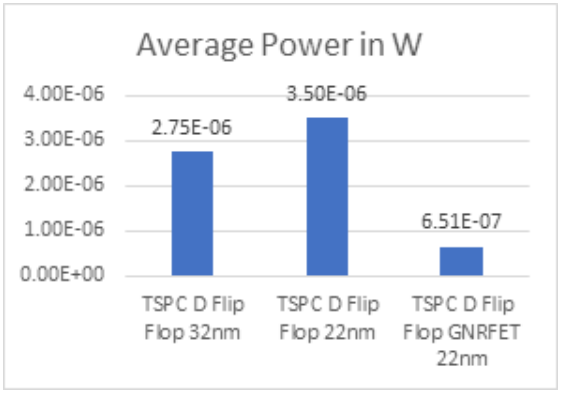

Figure 7: Average Power for 32nm and 22nm TSPC DFF MOS and GNR

Figure 7 shows that the TSPC DFF GNR based average power is lowest and 22nm MOS highest, which are the short channel consequences.

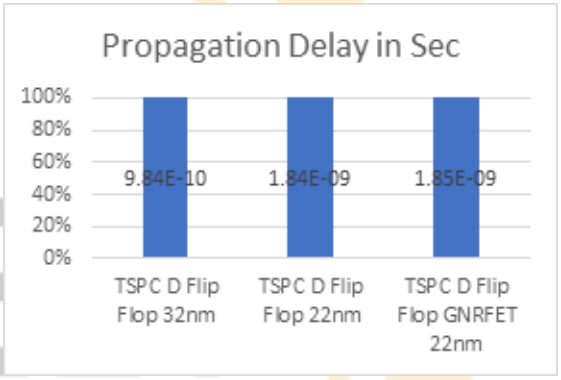

Figure 8: Delay for 32nm and 22nm TSPC DFF MOS and GNR

The delay case of GNRFET 22nm is considered to be the lowest on a single TSPC circuit in figure 8.

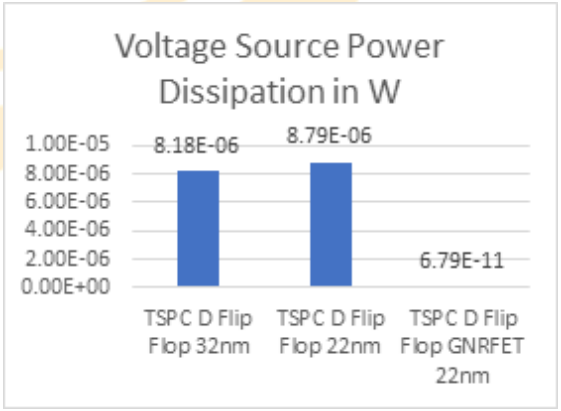

Figure 9: Voltage Source Power Dissipation for 32nm and 22nm TSPC DFF MOS and GNR

In Figure 9, the dynamic TSPC circuit based on GNRFET shows the lowest voltage power dissipation.

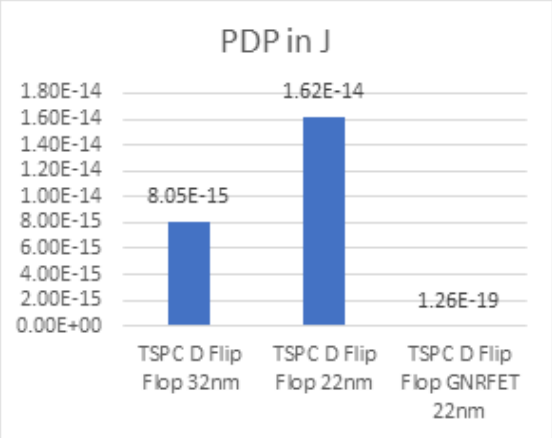

Figure 10: PDP for 32nm and 22nm TSPC DFF MOS and GNR

Figure 10 shows the PDP in DFF TSPC GNR as lowest and in MOS TSPC 22nm as highest.

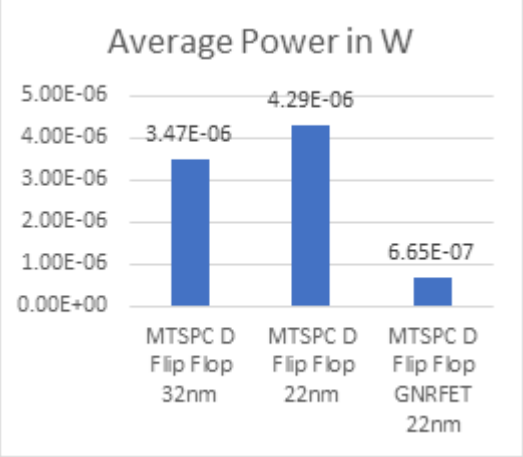

Figure 11: Average Power for 32nm and 22nm Modified TSPC DFF MOS and GNR

In the case of the upgraded TSPC D flip flop 22nm setup the average power and delay is also low in figures 11 and 12.

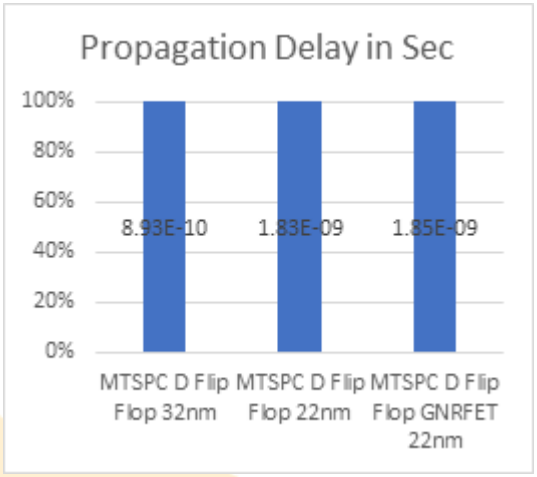

Figure 12: Delay for 32nm and 22nm Modified TSPC DFF MOS and GNR

In figures 13 and 14, 22nm modified are the lowest power and energy dissipation. DFF of TSPC.

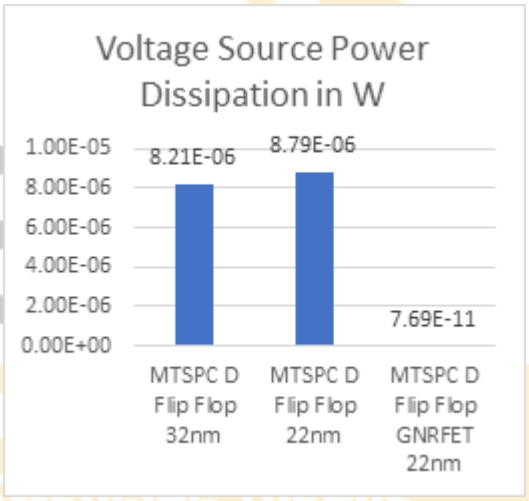

Figure 13: Voltage Source Power Dissipation for 32nm and 22nm Modified TSPC DFF MOS and GNR

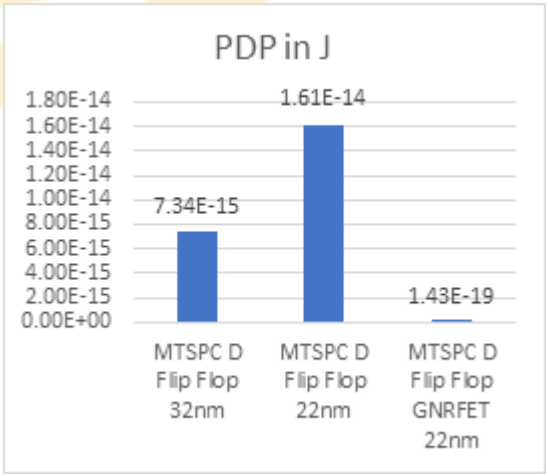

Figure 14: PDP for 32nm and 22nm Modified TSPC DFF MOS and GNR

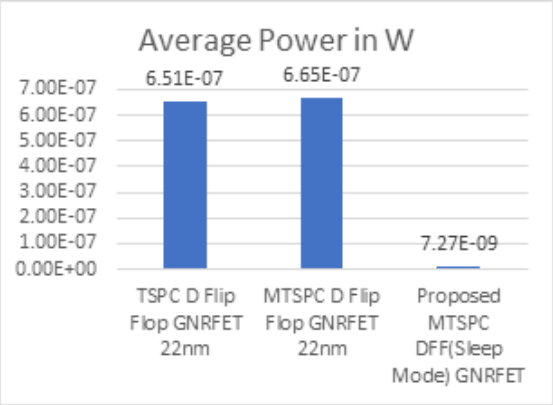

Figure 15: Average Power for 32nm and 22nm Proposed Sleep Mode based Modified TSPC DFF GNR

In the proposed TSPC D Flip Flop, the average capacity is better than in figure 16.

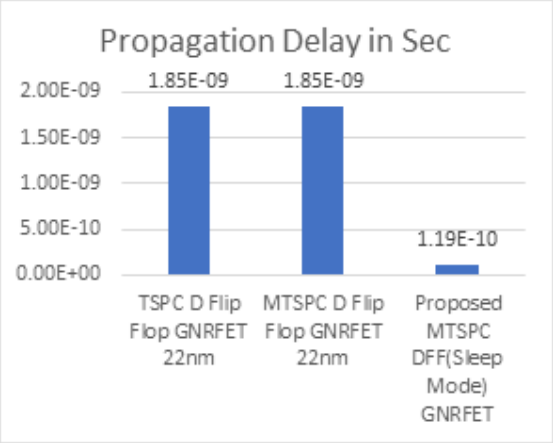

Figure 16: Delay for 32nm and 22nm Proposed Sleep Mode based Modified TSPC DFF GNR

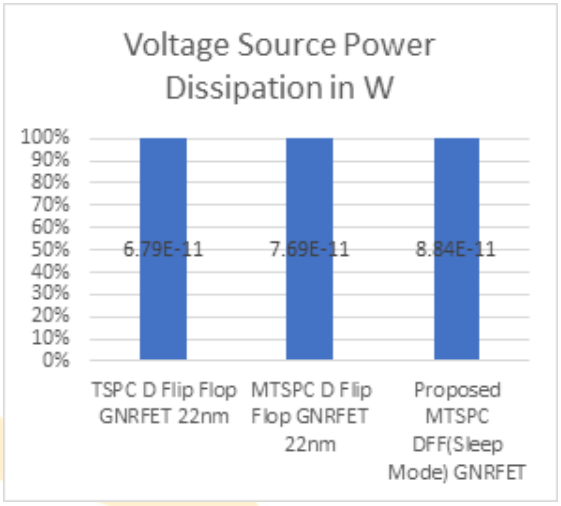

Figure 17: VSPD for 32nm and 22nm Proposed Sleep Mode based Modified TSPC DFF GNR

The power supply for all GNRFET-based circuits is almost the same, as shown in Figure 17, and this does not have a negative effect on the proposed circuit.

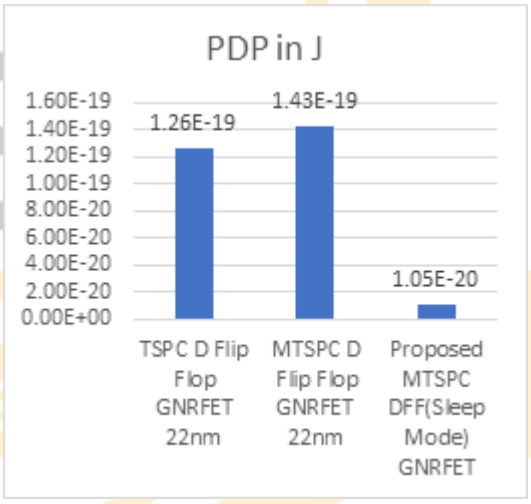

Figure 18: PDP for 32nm and 22nm Proposed Sleep Mode based Modified TSPC DFF GNR

In figure 18, the proposed circuit has the lowest PDP of 22nm of technical contributions in all GNR based circuits compared to the proposed.

Conclusion

The results of the simulation show that making use of Sleep Mode reduces the typical amount of power consumed, increases the amount of time it takes for energy to be dissipated, and prolong the length of time it takes for the delay to accumulate. The voltage source power dissipation is almost same for each and every one of the GNRFET-based circuits. The results of the experiment were verified by both

HSPICE and Avanwaves respectively. With a reduction of 97.9% of time, the power dissipation has been cut down to 99.9%, and the voltage source PDP has been finely adjusted to about 90%. The average power has increased by a growth of 96.55%. In combination with the GNRFET Sleep Mode technology, the Dynamic D Flip Flop adjustable circuit, which offers advantages such as low power consumption and high-speed optimization, may be put into use.

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