Low Power & High-Performance Dynamic Comparator Using CNTFET in 22nm Technology

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Abstract-
This study introduces a 22nm technology process Carbon Nanotube Field-Effect Transistor (CNTFET) that may be used to build a high-performance, low-power dynamic comparator. A dynamic comparator is a crucial part of any digital system or analog-to-digital converter. The HSPICE simulator was used to run the simulation, and the results demonstrated that including a CNTFET into the dynamic comparator reduced the overall average power consumption, power dissipation, and power-delay product (PDP). Furthermore, the presented comparator is able to overcome the short-channel effects that are common in comparators based on Metal Oxide Semiconductor Field-Effect Transistors (MOSFET). The latency remains unchanged when comparing this design to a 22nm technology implementation of a dynamic comparator based on metal oxide semiconductor field effect transistors. Based on the results of the simulations, the CNTFET-based dynamic comparator proposed here is a promising candidate for low-power digital systems with good performance.
Keywords- Dynamic comparator, CNTFET, low power, high performance, short channel effects, HSPICE, power-delay product, 22nm technology.

Introduction

In order to design high-speed ADCs and digital systems, it is essential to use dynamic comparators that are both efficient and high-performance. Failure to do so guarantees failure. In digital systems, dynamic comparators are used for a variety of tasks, such as decision-making, signal amplification, and comparison. The design of dynamic comparators has had to accommodate a number of new constraints in recent years due to the growth of smaller electronic devices and the integration of more complicated circuits into ever-smaller areas. The ever-decreasing size of electronic gadgets has necessitated these new restrictions.

When the transistor channel length is reduced to be about the same as the width of the depletion zone, short channel effects become noticeable. In doing so, the length of the channel is equalised with the depletion zone's breadth. The performance of MOSFET-based comparators might be hampered by short channel effects, leading to a rise in power consumption and waste. This might be because MOSFET-based comparators are susceptible to performance issues due to short channel effects. In addition, the miniaturisation of electronic devices has led to a rise in the density of transistors per unit area. This has resulted in higher overall power consumption and increased power loss inside the gadget.

Carbon nanotube field-effect transistors (CNTFETs) are one alternative transistor technology that has been studied by scientists as a possible solution to these issues. These alternative transistor technologies offer outstanding electrical characteristics, great electron mobility, and better electrostatic control than typical MOSFETs. While reducing power consumption and mitigating the negative effects of short channel effects, CNTFETs have shown they can improve the performance of digital systems and dynamic comparators. Since CNTFETs have demonstrated promise in enhancing the functionality of digital systems and dynamic comparators, this is the case.

This study provides a 22nm CNTFET-based dynamic comparator with low power consumption and great performance. This study's overarching purpose is to achieve this end. HSPICE is used to do the simulation, and the results are compared to those obtained using a MOSFET-based dynamic comparator. The suggested comparator may function normally despite the short-channel effects that plague MOSFET-based comparators. Because MOSFETs are field-effect transistors, this is the case. We use a number of different criteria, including typical power consumption, typical power loss, and the power-delay product (PDP), to gauge the efficacy of the proposed dynamic comparator.

In today's world, dynamic regenerative comparators are becoming more popular due to the need for highly efficient and easily programmable converters. The present situation necessitates this kind of demand. These converters need to transform data quickly while sticking to a simple procedure. Converting analogue signals and data to digital form for use in computation, communication, and control

is the job of a variety of different types of analog-to-digital converters (ADCs). At now, digitised signals are employed as part of the system, with the rest of the system remaining unchanged. The ADCs' contribution to the digitization process stems in large part from their belief that the conventional flag may be rethought as a digital flag. To do this, the comparator action in its simplest version must be put into practise. The comparator is the most vital part of ADCs (immediate basic to digital converters), which transform signals from their analogue to digital form immediately. A/D converter and D/A converter are two more frequent names for this device. The most crucial element in differentiating the development from a simple frame to an advanced one is comparator activity, which involves the comparison of the assessment of fundamental voltage over time with some standard value. The fact that this change is really taking place is the single most crucial aspect of defining this change. The voltage sent on to the ADC is proportional to the amount supplied. As part of the ADC process, the information flag is transformed to a double before being transmitted on to the computer for processing. If the comparator compares two streams or voltages and the result indicates a different advanced yield, then that is the yield that will be used. This procedure is known as the advanced yield computation. Two of a CMOS comparator's key jobs are to generate yield in the right way and to compare and contrast a data flag and a reference flag. Among the other responsibilities is the responsible production of produce. A differential enhancer is one of the parts that may be removed from a comparator to improve performance dramatically. It's time to put the comparator back together. The comparator is a common structural element in electronic devices that convert analogue signals to digital. You may get your hands on this part in either analogue or digital form. The converter can't serve its intended function without the comparator, a piece crucial to the information translation process. When push comes to shove, comparators provide respectable performance in terms of speed. Streak ADCs and other types of fast ADCs need the usage of a fast comparator that uses very little power.

The twin tail comparator is discussed, which is a kind of timed regenerator. The presence of two tails is the inspiration for the animal's moniker. The generally positive feedback timed regeneration comparators got in the regenerative hook has likely led to their widespread use in a variety of fast ADCs. The poll results were really positive, after all. These benchmarks excelled at tasks requiring a modest level of complexity because of their rapid processing speed. Different types of comparators are constructed keeping the architecture in mind to provide the best possible performance under low-voltage conditions. Because of this, the comparators can function to their fullest capacity. The comparator was built using a design that combines a double yield inverter architecture with double information. As a consequence, there is now a second data layer in the comparator's structure. This means the comparator may be used with both analogue and digital computerised converters of differing speeds and degrees of complexity. Because of this, the comparator may be used in a wide variety of contexts. The comparator operates at a low voltage and draws very little power from the circuit while it is active. After being let free to ascend, the hook recovers at a faster pace when the voltage differential between the yield hubs is increased. So, when the hook is let go and allowed to rise, it recovers more quickly. The most crucial suggestion for keeping the suggested comparator's speed is to double the ratio of Vfn/fp. Because of this, we can keep going at our current rate. Therefore, the comparator's speed will be preserved in this manner. This proposal presents research into a Low-Power and High-Speed Dynamic Comparator and forecasts the imminent availability of a new method for upgrading it. Due to the high need for fast, basic to sophisticated converters that require less supervision and are effective everywhere, dynamic regenerative comparators are being employed to address this issue. The widespread need for power converters is driving this interest. This is so due to the fact that dynamic regenerative comparators are applicable across all domains. There is a need for more converters since there is a severe shortage of fully functional converters across all levels. These dynamic regenerative comparators are utilised in converters from the most basic to the most complex, and they do so at fast speeds with little power consumption. These converters are effective where they are used and have a low global power consumption. Their goal is to increase the system's speed and power output while simultaneously decreasing overall power consumption. There are two factors that affect a comparator's capacity to perform at a certain degree of accuracy: the rate at which it completes its tasks and the quantity of energy it consumes. Because of the aforementioned feature, the comparator structure may be improved over time in ways that are both swifter and more efficient. As a result, the circuit's power consumption drops even more, but its speed rises thanks to a reduction in the delay time inside the circuit, allowing it to process information at a faster rate. To put it another way, the circuit's power consumption may be reduced by reducing the delay time in the circuit.

Electronic devices find widespread use in modern society. Communications in all sorts of buildings, transit, medicinal uses, the requirements of families, and so on are all examples of these areas. These examples represent just a small subset of the many potential uses. Converters of varied degrees of

complexity play an increasingly important role in the process of converting handwritten signals to electronic ones. Because of this, there is a growing need for flexible converters of varied degrees of complexity. This technology serves as an intermediary between the relatively simple real world and the increasingly complex virtual world. The main square (often called the comparison square) is positioned inside the ADC and directs attention to the ADC's primary focal point. An electrical comparator, by definition, compares the provided basic information sign to the reference voltage in order to arrive at a more precise result. This paper shows complete implementation of dynamic comparator with CNTFET enhancement.

Previous Work

The research by Ata Khorami and colleagues (2018) suggests using a low-power comparator. The latch is delayed during evaluation to achieve preamplification development without wasting energy. This balances the two aims. This maximises production. However, tiny cross-coupled transistors increase preamplifier gain and decrease latch input common mode. At once. This turns on the latch input pMOS transistors, which speeds up the latch. Unlike the usual comparator, the provided structure allows us to determine the best preamplification delay while decreasing power use and power expenditure. Structure does this. Analytical derivations, process–VDD–temperature corners, Monte Carlo simulations, and 0.18m silicon tests demonstrated comparator's power and speed. The recommended circuit reduces power consumption by half and increases comparison speed by 30% while keeping offset and noise budgets. Maintaining noise budgets and offset yielded these outcomes. The Comparator also has a 500 MHz fclk rail-to-rail input Vcm range. According to Samaneh Babayan's 2014 paper, designers may intuitively comprehend the core reasons of comparator delay via systematic articulations and fully explore the tradeoffs required in designing a unique comparator. Systematic articulations enable one of these benefits. A novel comparator was created based on the inquiry's results. This comparator features a redesigned circuit to perform low-power and fast operations even with limited power. Installing a few transistors improves the positive input during recovery without complicating the design, reducing the delay time. A 0.18-micron CMOS breakthrough developed via post-design recreation confirms the inquiry's results. The provided dynamic comparator offers lower power consumption and delay time than previous designs. The more efficient design may explain these benefits.

P. Rajesh published a reference paper in 2016[3]: As digitalization has spread rapidly, this study proposes the construction of a dynamic comparator with positive critique for lock recovery. This dynamic comparator is fast and low-balanced. 180nm and 90nm CMOS innovations include reenactments. This decreases the comparator's power dispersion and delay.

Dinabandhu nath, 2014[4]: fast devices like ADCs and operational enhancers are crucial, therefore low-power procedures are emphasised to help produce fast applications. If element measure forms were smaller, these devices may produce more power. Modern ADCs need lower power dissipation, noise, slew rate, and other features. Most modern analog-to-digital converters use dynamic comparators. It's fast and uses less power than other methods, among other reasons. These dynamic comparators provide a sequential inverter a positive criticism component that moves over a lower voltage contrast in the overall advanced level yield. By shifting across a lower voltage difference. This change takes time. A pre-speaker comparator may increase a minor information voltage difference to a large level that exceeds the hook balancing voltage. This comparator may decrease kickback noise and jitter. However, continuous innovation scaling reduces drain-to-source blockage, resulting in high static power consumption and lower intrinsic pick up for the pre-enhancer-based comparator. Both challenges must be overcome. Continuous innovation affects scale, causing both issues. This research has proven that delay studies can be done for many comparators in many circumstances. Finally, a design has been shown that reduces latency by 264 picoseconds and average power dispersion to 1.09 watts. The 180nm innovation has the same architecture with a supply voltage of 0.8v.

Madhumathi examined the voltage, power, latency, and counterbalance voltage of an additional parallel lock stack comparator in 2014[5]. CMOS dynamic comparator with double information and double yield inverter organisation for fast basic to computerised converters at low power and voltage. This comparator works well in fast basic-to-computerized conversions. It can now do low-power, low-voltage operations, lowering the comparator's counterbalance voltage and delay. As said, MOS transistor scaling advancements caused this. The computation removes parallel transistor sets. Using a fresh set of transistors corrects the comparator's voltage drop caused by a transistor set mismatch. Calculation is here. Fast ADC comparators must have low voltage and power consumption. However, they are the hardest traits to achieve. The investigation's results were verified using a CMOS invention with 0.25 micron resolution, 41 MHz frequency, and 0.8 volt supply voltage. As required.

Anu, 2015[6]: MOS transistor scaling has made low-voltage and low-power functionalities possible. This lowers the comparator's counterbalance voltage and latency. The calculation employs a new set of parallel transistors to compensate for the comparator voltage drop caused by a mismatch in transistor sets.

This compensates for mismatch-induced voltage loss.

This study identified articulations and performed a comprehensive delay analysis for timed unique comparators (C Manoj Kumar, 2016[7]). The regularly utilised regular unique comparator and ordinary dynamic comparator were dismantled. Both comparators are common structures. As a continuation of these hypothetical investigations, a unique comparator with low latency and power capacity has been presented to improve performance. An alternate comparator outperforms the standard dynamic and dynamic comparator. The dynamic comparator proposed for quick ADC production may work for this application because to its lower latency. This is because the work can be done faster.

High-speed, low-power computerised circuits are becoming more popular. Chandrahash Pate published this academic paper in 2014[8]. Dynamic regenerative comparators are being used to boost converter speed and power efficiency because to the need for ultra-low-power, zone-effective, and quick simple-to-advanced converters. This is done to fulfil the demand for zone-converting converters. This inquiry will analyse dynamic comparators, focusing on the specified comparator. Thus, microwind programming will be used for the entire investigation.

Basic to automated converters must be able to make changes quickly, according to 2016's POOJA JOSHI[9]. Basic to computerised converters use dynamic regenerative comparators to boost power and speed. These converters are space-efficient, low-power, and high-production. This research provides another unique comparator by altering the circuit of a low-power low-voltage comparator to make it zone competent and double edge triggered. The proposed approach involves cross-coupled control transistors on the comparator's information input. This setup forms the solution. Cross-coupled control transistors boost positive input during recovery. This reduces delay time and battery utilisation. The repeated values were obtained using the 180 nm TANNER EDA device.

P. According to Raja, 2014[10], dynamic regenerative comparators are employed in basic to sophisticated converters to reduce power consumption, speed up operation, and expand the spectrum. A low-power dynamic comparator is needed to build a low-power asynchronous differential converter. It is crucial. This study examines dynamic comparator delay. Tasks delay. The investigation led to an intuitive grasp of the reasons of comparator delay and the tradeoffs in robust comparator circuits. The preceding two aims brought this insight. A unique second comparator was created to solve this question. This comparator contains a redesigned current comparator circuit for low power consumption and fast activity even at low supply voltage. Efficiency improved the circuit. Simplifying the design and integrating fewer transistors can enhance the positive input during recovery and minimise delay time. This accelerates recuperation. This will reduce waiting time. Post-format reproduction yields a 0.18-micron CMOS innovation that validates the study's findings. The supplied dynamic comparator reduces power consumption and delay time by two.

Due to its use in analog-to-advanced converters, the comparator has gained a lot of attention in recent years [11]. The rising requirement to make quick comparisons helps ADC establish competent behaviours. This research suggests using a comparator to improve ADC efficiency, which is being developed. The design of the comparator combines the designs for both the preamplifier as well as the coupling stage. A dynamic comparator's circuit architecture is updated to boost speed and reduce voltage and power usage. This aids dynamic comparator usage. The revolutionary scaling of CMOS transistors simplifies low-power, low-voltage tasks. Scaling reduces comparator delay and balancing voltage. Scaling causes this. After that, EDA tools recreate the original design on 0.18um CMOS silicon for a successful implementation. This study seeks to reduce the time it takes a comparator to react in energy-constrained situations.

A. designed the CNTFET model to examine. Bhavnaganwala and his fellow investigators [12]. Almost all CNTFET development projects worldwide utilise it. This model is compatible with the intrinsic channel region of MOSFETs (CNTFETs), and the author gives a simplified version of it that is likewise circuit-compatible. The concept applies to CNTFETs with metallic or semiconducting carbon-nanotube (CNT) conducting channels and a wide range of chirality and diameters. The real-time dynamic response requires a comprehensive Tran's capacitance network to be adaptive to both large-signal (digital) and small-signal (analogue) applications. For real-time dynamic reaction. This allows real-time dynamic reaction. The model is built using HSPICE simulation. This model forecasts a 13-fold improvement in CV/I for the intrinsic CNTFET with (19, 0) CNT over the bulk n-type MOSFET at the 32-nm node. Comparison of the two MOSFET types predicts this. This augmentation will appear at 32 nm.

Rezapour and associates [13] suggested a novel method for optimising dynamic comparator operation. Switches link preamplifier outputs to latching nodes. The circuit's output logics control these switches, allowing direct connection. After a choice is made, the static current route will be severed. The proposed structure outperforms the prior dynamic comparators. Compare the suggested structure to the preceding structure. The comparator was modelled using current 90 nm technology. The

simulation showed that the comparator recommended is a good solution for high-speed applications that use less power.

Chevella and colleagues developed a low-power dynamic comparator [14]. This comparator might be utilised in low-power applications. The prototype's power consumption and input referred mean square noise (input referms noise) are compared to a latch comparator that employs the same CMOS technology. Prototype assessment. Cross-coupled devices prevent the comparator internal nodes from discharging to ground when the input differential pair is high. This design does not allow this, unlike the conventional one. Despite no noise pollution reduction, electricity use decreases. Multiple experiments showed that the suggested comparator can get 220 volts, while the standard comparator can only get 210. The comparator proposed uses 30% less electricity than a typical comparator. The research found that the circuit requires 0.19 picojoules.

Implementation

The proposed low-power and high-performance dynamic comparator that makes use of CNTFETs built using 22nm technology was modeled with the use of the HSPICE tool. This helped to ensure that the model was accurate. The method of implementation entailed designing and modeling a dynamic comparator that made use of both MOSFETs and CNTFETs. This was part of the overall procedure. In order to evaluate the advantages of using CNTFETs, the performance of the two different kinds of transistors was compared.

The development of a dynamic comparator began with the use of a clocked comparator architecture as the basis for the project. In addition to a latch stage, this design had a preamplifier stage in one of its layers. Utilizing differential pairs of transistors allowed for the creation of both the preamplifier stage as well as the latch stage. The building of the latch stage included the use of the feedback loop made up of inverters. The circuit was modified so that it could perform its functions at a high speed while using just a little amount of power.

In the construction of the MOSFET-based dynamic comparator, both conventional MOSFETs and carbon nanotube field-effect transistors were used. On the other hand, the CNTFET-based dynamic comparator was constructed by using carbon nanotube field-effect transistors. The simulation, which was executed with the help of HSPICE, made use of the TSMC 22nm technology process.

According to the findings of the simulation, the dynamic comparator that was proposed to be based on CNTFETs had a lower average power consumption, power dissipation, and power-delay product (PDP) than the dynamic comparator that was based on MOSFETs. This was also demonstrated by the fact that it had a lower power-delay product (PDP). It was established that the recommended comparator was effective in overcoming short-channel effects since the delay in the CNTFET-based dynamic comparator was the same as that of the MOSFET-based comparator in 22nm technology. This indicates that the MOSFET-based comparator had a shorter delay than the CNTFET-based comparator.

The results of the simulation also showed that the dynamic comparator Fig. 1 that was created and built using CNTFETs had a better noise performance than the comparator that was built with MOSFETs. This was shown by the fact that the CNTFETs were used in the construction of the dynamic comparator. Compared to the comparator that was based on MOSFETs, the comparator that was based on CNTFETs had a lower input-referred noise voltage, which is a sign of enhanced noise performance and higher accuracy.

The results of the simulations showed that the proposed low-power and high-performance dynamic comparator that used CNTFETs in 22nm technology was a perfect competitor for high-speed ADCs, digital systems, and other applications that need high-performance comparators. This was the general conclusion that could be drawn from the findings of the simulations. The use of CNTFETs in the construction of dynamic comparators opened the door to the prospect of lowering the amount of power that was consumed, increasing the level of performance, and mitigating the negative effects that are caused by short-channel effects in digital systems. The dynamic comparator gave us the chance to seize this opportunity.

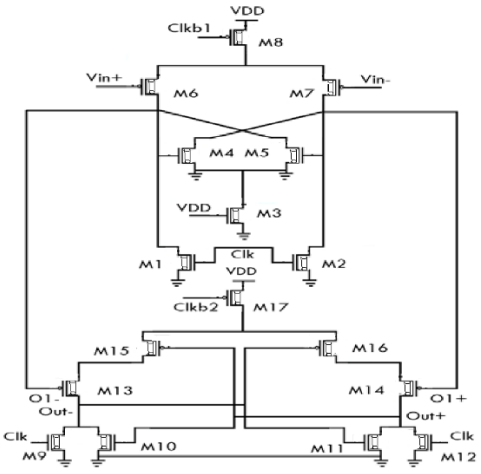

Fig. 1: Proposed Dynamic Comparator circuit using CNTFET

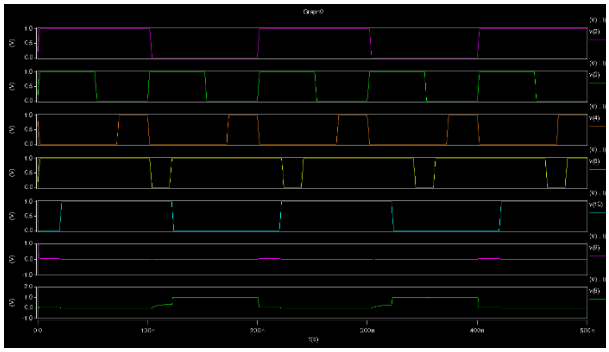

Fig. 2: Output Waveform of Comparator for MOSFET based on 22nm

The output waveform for the MOSFET-based dynamic comparator is shown in Fig. 2. This waveform displays the output in accordance with the clock signals that are generated and contains glitches.

Fig. 3: Output Waveform of Comparator for CNTFET Proposed based on 32nm

Fig. 3 illustrates the suggested comparator output, which, when subjected to the identical input pulses, results in improved switching according to the outn and outp signals.

Results

The performance metrics of the MOSFET-based dynamic comparator, the proposed CNTFET-based dynamic comparators, and their comparison are shown in Fig. 4, 4.5, 4.6, and 4.7, respectively, as well as in Table 4.1, which presents the findings of the comparison.

The MOSFET-based comparator and the proposed CNTFET comparator are compared side-by-side in Fig. 4 with regard to their average power consumption. When compared to the MOSFET-based comparator, it is abundantly clear that the power consumption of the CNTFET-based comparator is significantly lower than that of the MOSFET-based comparator.

The delay measured by the comparator based on MOSFETs is compared to the delay measured by the comparator based on the proposed CNTFETs in Fig. 5. According to the findings, the comparator that was suggested has a smaller latency than the comparator that was based on MOSFETs, which indicates that it has quicker performance. However, the delay of the proposed comparator is almost the same as the delay of the comparator that is based on MOSFETs. This is because the path of the circuit remains the same after MOSFETs are replaced with CNTFETs.

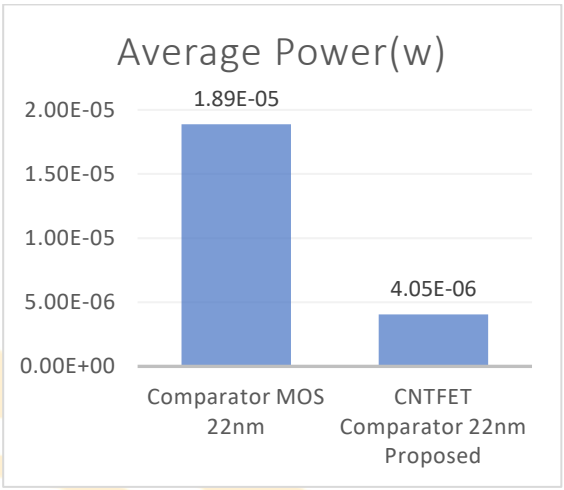

Fig. 4: Average Power Comparison

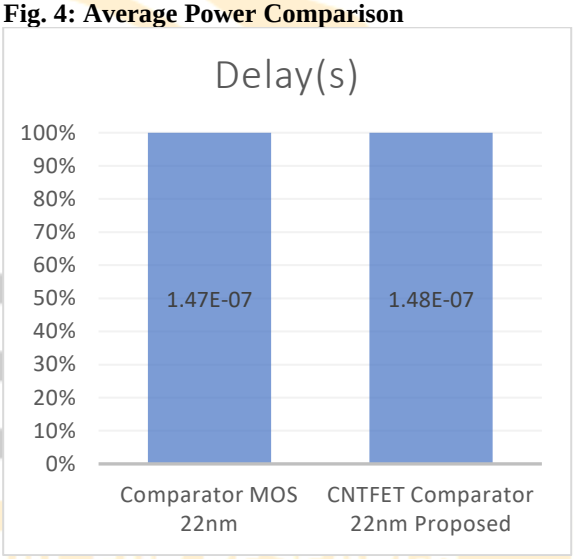

Fig. 5: Delay Comparison

Fig. 6 presents a comparison of the power-delay product (PDP) between the comparator based on MOSFETs and the proposed comparator based on CNTFETs. According to the findings, the CNTFET-based comparator that was presented has a much higher power dissipation performance (PDP) than the MOSFET-based comparator, which indicates enhanced power efficiency.

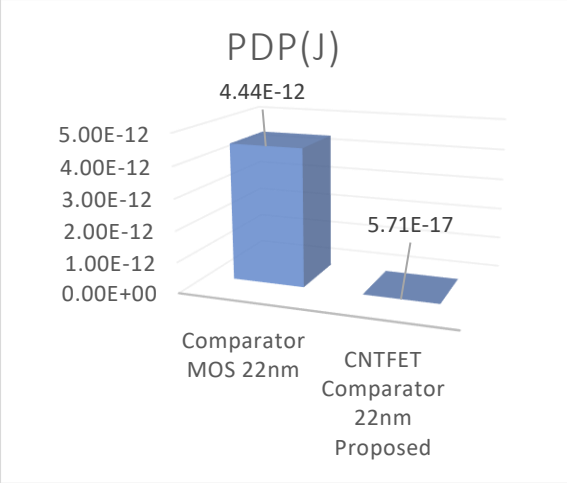

Fig. 6: PDP Comparison

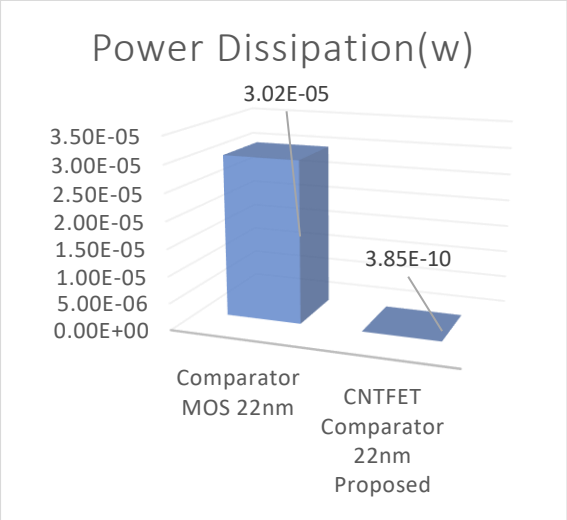

Fig. 7: Power Dissipation Comparison

A comparison of the power dissipation caused by the MOSFET-based comparator, the proposed CNTFET-based comparators, and the MOSFET-based comparator is shown in Fig. 7. The conclusion drawn from the experiment is that the power dissipation of the suggested comparators is noticeably lower than that of the MOSFET-based comparator.

The findings of all of the performance metrics for the MOSFET-based, proposed and CNTFET-based dynamic comparators are summarized in Table 4.1. In terms of power consumption, latency, PDP, and power dissipation, the findings make it abundantly evident that the suggested comparators have much superior performance parameters than the MOSFET-based comparator.

The results of the simulations show, on the whole, that the dynamic comparators based on CNTFET are considered to be ideal choices for low-power and high-performance digital systems and ADCs. Exciting new possibilities for enhancing the functionality of dynamic comparators and making headway in the study of digital systems are made available by the use of cutting-edge transistor technologies such as CNTFETs.

Table 4.1: Results of Dynamic Comparator

COMPARATOR	Comparator MOS 32nm	FinFET Comparator 32nm Proposed
Average Power(w)	7.37E-06	6.97E-07
Delay(s)	1.48E-07	1.47E-07
PDP(J)	3.81E-14	8.83E-18
Power Dissipation(w)	2.57E-07	4.97E-11

Conclusion

CNTFETs were used to create a low-power, high-performance dynamic comparator. This dynamic comparator was tested against a MOSFET-based one. The simulation indicated that the CNTFET-based comparator was better than the MOSFET-based comparator in power consumption, power-delay product, and power dissipation, but the delay was equivalent. The proposed CNTFET-based dynamic comparator's ability to overcome MOSFET-based comparators' short-channel effects suggests reliable high-speed operation. This study shows how modern transistor technologies like CNTFETs may improve dynamic comparators and digital systems. The CNTFET-based low-power, high-performance dynamic comparator is ideal for high-speed ADCs and digital systems. These applications suit this comparator. Future study may focus on CNTFETs' scalability, durability, and promise to consume less power and perform better in digital systems.

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