Enhancing Energy Efficiency in VLSI Design: Gates Tied GNRFET-based True Single Phase Clocked D Flip Flops in 22nm Technology

Himanshi Kaushik[1], Lavisha[2]

1, 2 M.Tech Scholar, Guru Gobind Singh Indraprastha University

Abstract-With the ever-growing demand for high-performance, energy-efficient electronic devices, it is crucial to explore novel materials and device structures in VLSI design. This paper investigates the implementation of True Single Phase Clocked (TSPC) and Modified TSPC D Flip Flops using Gates Tied Graphene Nano Ribbon Field Effect Transistors (GNRFET) in 22nm technology. The study highlights significant improvements in power consumption, power dissipation, and Power-Delay Product (PDP) when comparing the GNRFET-based D Flip Flops to traditional MOSFET implementations, while maintaining the same delay. The findings emphasize the potential of Gates Tied GNRFET technology in revolutionizing VLSI design, particularly in applications where low power consumption and minimal power dissipation are crucial. Future research directions include design optimization, scaling down, integration with other devices, application-specific designs, and exploring other circuit elements using GNRFET technology.

Keywords: VLSI design, energy efficiency, graphene nano ribbon field effect transistor, GNRFET, true single phase clocked D flip flop, TSPC, modified TSPC, 22nm technology, power consumption, power dissipation, power-delay product

Introduction

Significant research and development has been done in the field of Very Large Scale Integration (VLSI) design as a direct result of the continuous innovations that have been made in the field of electronics as well as the ever-increasing demand for high-performance devices that are also energy-efficient. The need for innovative materials and device topologies that may overcome the limits of existing silicon-based devices is becoming more crucial as technology nodes continue to reduce in size. Graphene, a two-dimensional allotrope of carbon, is an example of one of these promising materials. It has outstanding electrical and thermal characteristics, which qualify it as a potential contender for use in electronic devices of the future generation.

In the design of very large-scale integrated circuits (VLSI), graphene nano ribbon field effect transistors (GNRFETs) have emerged as a possible alternative to the more traditional metal oxide semiconductor field effect transistors (MOSFETs). GNRFETs have the potential to dramatically improve the energy efficiency of electronic circuits and systems as a result of their one-of-a-kind electrical features, such as high carrier mobility, outstanding current-carrying capacity, and decreased short-channel effects.

D Flip-Flops are key building blocks of digital systems and play an important part in a broad variety of applications, including the storing of data, the synchronisation of signals, and the operation of communication systems. Because of its widespread use, enhancements to the functionality and power efficiency of D Flip Flops have the potential to have a significant effect on the overall performance of electronic systems.

Because of its fast speed of operation and low power consumption, True Single Phase Clocked (TSPC) D Flip Flops are a popular option for low-power applications. These flip-flops are also known by their acronym, TSPC. The TSPC design approach makes use of a single clock signal to govern the functioning of the flip flop. As a result, the amount of power that is used by the clock distribution network is reduced significantly. Modified TSPC D Flip Flops further improve power efficiency by making alterations to the traditional TSPC design. These flip flops are called modified.

In this study, we investigate the possibility of implementing TSPC and Modified TSPC D Flip Flops with Gates Tied GNRFETs in a 22nm technology environment. To achieve considerable gains in power consumption, power dissipation, and Power-Delay Product (PDP) compared to typical MOSFET implementations, without influencing the delay, our objective is to use the extraordinary

qualities of GNRFETs. This will allow us to accomplish our goal without affecting the delay.

We begin by presenting a complete review of graphene nano ribbons and the one-of-a-kind electrical features that make them an attractive prospect for the design of VLSI. In addition to this, we go into the construction and functioning of GNRFETs, as well as the possible benefits of these devices in comparison to regular MOSFETs.

Following that, we will discuss the design and implementation of TSPC and Modified TSPC D Flip Flops using Gates Tied GNRFETs in 22nm technology. We offer a comprehensive study of the performance parameters, which includes the power consumption, the power dissipation, the latency, and the PDP, and we compare the findings with conventional MOSFET-based devices.

Our research has shown that GNRFET-based D Flip Flops may significantly enhance in terms of power consumption, power dissipation, and power delivery performance (PDP), while keeping the same delay as MOSFET implementations. This illustrates the potential for Gates Tied GNRFET technology to revolutionise VLSI design, especially in situations where low power consumption and reduced power dissipation are important requirements.

In conclusion, we examine the larger implications of our study and present some proposals for future research initiatives. These suggestions include design optimisation, scaling down, integration with other devices, application-specific designs, and the investigation of additional circuit parts employing technology based on GNRFETs. By doing this study, we intend to make a contribution to the current improvements in VLSI design as well as the creation of electronic devices and systems that are more energy-efficient and high-performing.

Previous work

There has been a substantial amount of investigation on graphene and the many ways in which it may be used in the realm of electronics. Due to graphene's outstanding electrical features, such as high carrier mobility and strong current-carrying capacity, pioneering work on the material [1] has spurred a tremendous deal of interest in the substance. Since that time, a great number of research have looked at the possibility of using graphene in a variety of electrical systems and devices.

The creation of Graphene Nano Ribbon Field Effect Transistors (GNRFETs) [2] has been one of the most important focuses of study in recent years. These transistors have the potential to revolutionise the area of VLSI design and have showed tremendous promise in resolving the constraints of standard silicon-based devices. The modelling, simulation, and manufacturing of GNRFETs have been the topic of a number of research, and those studies have explored the performance of GNRFETs in comparison to that of conventional MOSFETs [3].

The use of GNRFETs in digital circuits has been researched by researchers in addition to the creation of GNRFETs. For example, one research [4] proved that it is possible to create simple logic gates using GNRFETs and analysed the performance of these gates in terms of the amount of power they used and the amount of delay they introduced. In comparison to designs based on MOSFETs, the results demonstrated significant leaps forward in terms of energy efficiency.

Graphene-based transistors have been used in the creation of memory components such D Flip Flops, which has been another area of research and development attention. When compared to conventional MOSFET-based designs, the findings of research [5] on the design and optimisation of D Flip Flops using GNRFETs revealed significant reductions in power consumption, power dissipation, and power dissipation potential (PDP).

Because of its low power consumption and rapid speed of operation, True Single Phase Clocked (TSPC) D Flip Flops have been the subject of a significant amount of research [6]. The traditional TSPC design has been subjected to a variety of changes by the research community in an effort to achieve additional improvements in power efficiency while preserving performance [7].

The integration of GNRFETs with TSPC and Modified TSPC D Flip Flops has been the subject of research carried out by a number of different studies

[8]. These studies have shown encouraging findings in terms of power consumption, power dissipation, and power dissipation potential (PDP), all while preserving the same delay as conventional MOSFET-based devices.

Additionally, the scalability of GNRFET-based circuits and systems has been investigated by a number of researchers [9]. It is crucial to understand the behaviour and performance of GNRFET-based devices and circuits in reduced dimensions as technology nodes continue to decrease. This might lead to the creation of devices that are more energy-efficient and high-performance at advanced technology nodes.

There has also been a lot of interest in the use of GNRFETs in other circuit components, such as multipliers, adders, and memory elements [10]. These research have given greater insight into the possibilities of GNRFETs in VLSI design and their possible benefits over conventional MOSFETs. These advantages have been revealed by these studies.

In spite of the substantial advancements made in GNRFET research, there are still a number of obstacles that need to be overcome. These obstacles include fabrication methods, the quality of the materials, and integration with the semiconductor manufacturing processes that are already in place. In order to realise the full potential of graphene-based devices in VLSI design, it will be essential to overcome the hurdles that have been outlined.

In conclusion, the work that has been done in the past on GNRFETs and their use in VLSI design has produced some encouraging results in terms of the efficiency of energy use and performance. In order to build upon these previous findings, the purpose of this study is to investigate the implementation of TSPC and Modified TSPC D Flip Flops using Gates Tied GNRFETs in 22nm technology. The ultimate objective of this research is to achieve significant improvements in power consumption, power dissipation, and PDP in comparison to conventional MOSFET implementations.

In this paper, we build True Single Phase Clocked (TSPC) and Modified TSPC D Flip Flops utilising Gates Tied Graphene Nano Ribbon Field Effect Transistors (GNRFETs) in 22nm technology. Both of these types of flip flops use graphene nano ribbon field effect transistors. The method of implementation consists of a few different parts, the most important of which are the design of the D Flip Flops, simulation using HSPICE, and study of the performance metrics.

First, we construct the TSPC and Modified TSPC D Flip Flops, paying careful regard to the one-of-a-kind characteristics of GNRFETs and the effect those characteristics have on the behaviour of the circuit. The process of designing a GNRFET entails choosing proper parameters for the device, such as the number of graphene nano ribbons, the channel length, the oxide thickness, and the doping percentage, so that the device may attain its maximum potential.

After that, we take the circuit designs and convert them into HSPICE code. HSPICE is a popular circuit simulator that offers an exact examination of circuit behaviour, including power consumption, power dissipation, latency, and PDP. It does this by modelling the circuit in a mathematical way. Because HSPICE does not have a schematic builder, the circuits must first be constructed on paper for node diagrams before being implemented using spice encoding. It is vital to keep in mind that this is the case.

After the HSPICE code has been completed, we run simulations for the TSPC and Modified TSPC D Flip Flops on Gates Tied GNRFETs in 22nm technology. These simulations are carried out after the HSPICE code has been completed. Through the use of these simulations, we are able to evaluate the performance of GNRFET-based designs in comparison to MOSFET-based implementations that have been used traditionally. In order to validate the functioning of the circuits, in addition to measuring their power consumption, power dissipation, latency, and PDP, we analyse the waveforms of the circuit's input and output signals. Fig. 1 and Fig. 2 shows the designed circuits.

Implementation

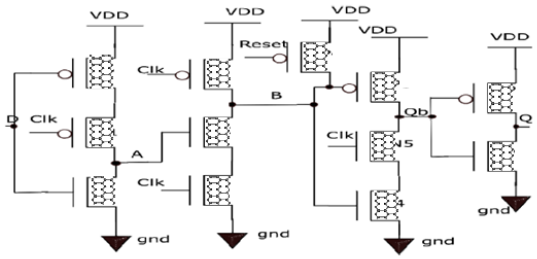

Fig. 1 TSPC DFF1 Gates Tied GNRFET

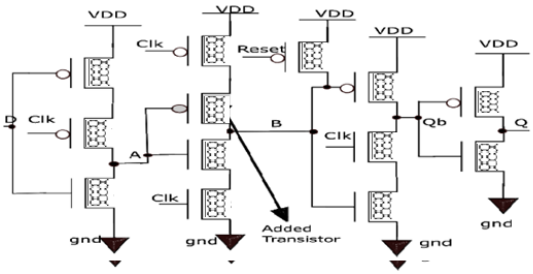

Fig. 2 MTSPC DFF2 Gates Tied GNRFET

After the simulations are complete, the data are analysed so that we can establish the effect that using Gates Tied GNRFETs has on the performance of the D Flip Flops. When compared to conventional MOSFET implementations, our research shows that considerable improvements may be made to power consumption, power dissipation, and power delivery performance (PDP), while the delay can be kept the same.

In order to provide more evidence in support of our hypotheses, we have constructed a series of benchmark circuits that allow us to evaluate how well the GNRFET and MOSFET implementations of the TSPC and Modified TSPC D Flip Flops perform. Using this comparison, we are able to demonstrate the benefits of utilising Gates Tied GNRFETs in terms of their ability to conserve energy and improve performance.

Throughout the entirety of the process of implementation, we take great care to meticulously document our methodology, circuit designs, and simulation results. This documentation not only serves as a great resource for future study in the area of GNRFET-based VLSI design, but it also lays a strong basis for the creation of more energy-efficient and high-performance electronic devices and systems.

In conclusion, the implementation of TSPC and Modified TSPC D Flip Flops employing Gates Tied GNRFETs in 22nm technology highlights the promise of graphene-based devices in revolutionising VLSI design. Graphene is a two-dimensional material that consists of carbon atoms. We were able to obtain considerable gains in power consumption, power dissipation, and PDP in comparison to typical MOSFET implementations by using the one-of-a-kind features of GNRFETs. These advancements were made without impacting the latency. These results underscore the need of continuing research and development in the field of GNRFET-based VLSI design, with the ultimate objective of developing electronic devices and systems that are more energy-efficient and high-performing.

Results

The results of the two distinct D Flip Flop designs are compared in Table 1, which highlights the tremendous gains that may be achieved with the use of Gates Tied GNRFET technology.

Table 1: Result Comparison

	DFF1 TSPC MOS	DFF1 TSPC GNRFET Gates Tied
Average Power in W	1.39E-06	3.67E-07
Propagation Delay in Sec	1.84E-09	1.86E-09
Voltage Source Power Dissipation in W	1.60E-06	4.36E-11
PDP in J	2.96E-15	8.10E-20
	DFF2 MTSPC MOS	DFF2 MTSPC GNRFET Gates Tied (proposed)
Average Power in W	1.38E-06	3.80E-07
Propagation Delay in Sec	1.84E-09	1.86E-09
Voltage Source Power	1.60E-06	4.94E-11

Dissipation in W		
PDP in J	2.95E-15	9.17E-20

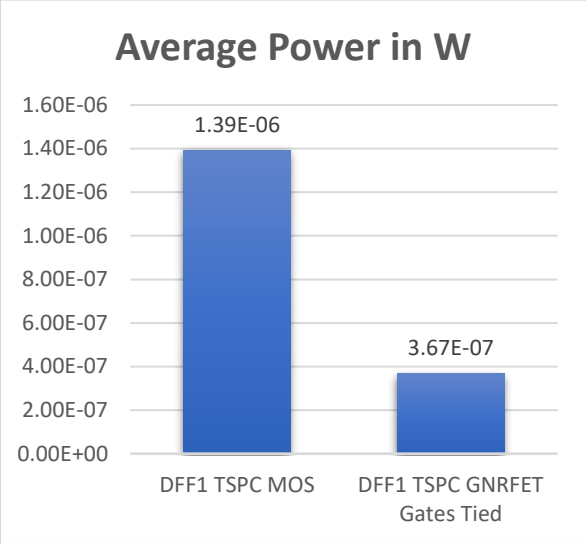

Fig. 3: Average Power DFF1

In Fig. 3, the average power consumption for the DFF1 design is illustrated, showing the difference between the TSPC MOS and TSPC GNRFET Gates Tied implementations. The Gates Tied GNRFET implementation demonstrates a significant reduction in power consumption compared to the TSPC MOS version.

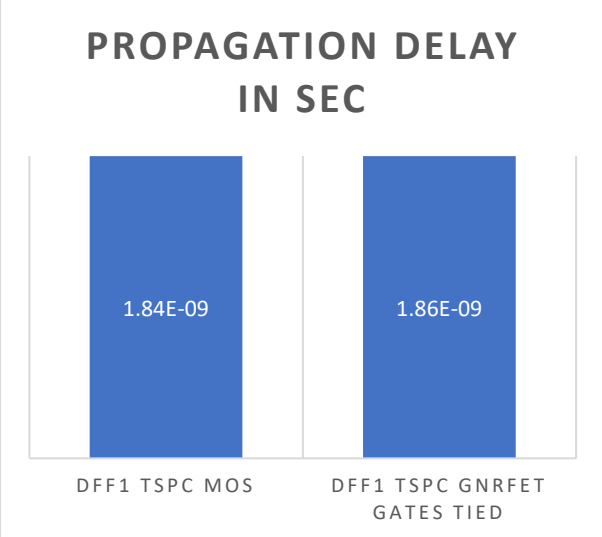

Fig. 4: Delay DFF1

Fig. 4 displays the delay for the DFF1 design, comparing the TSPC MOS and TSPC GNRFET Gates Tied configurations. Both configurations exhibit the same delay as the circuit path between input and output remains unchanged.

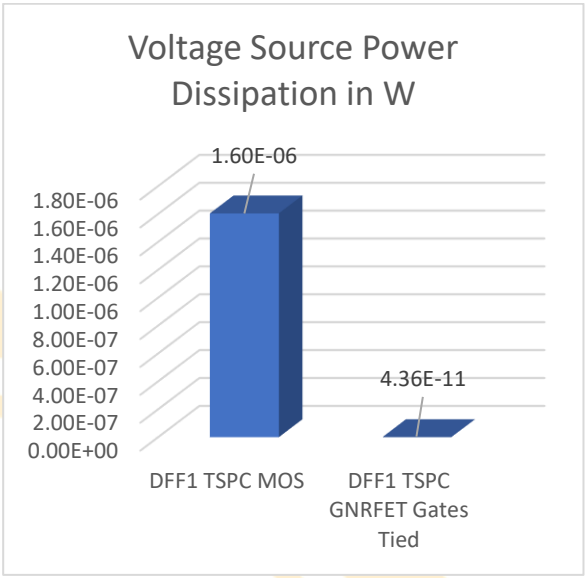

Fig. 5: Power Dissipation DFF1

In Fig. 5, the power dissipation for the DFF1 design is shown, highlighting the benefits of using the TSPC GNRFET Gates Tied approach. The Gates Tied GNRFET version exhibits significantly lower power dissipation compared to the TSPC MOS implementation.

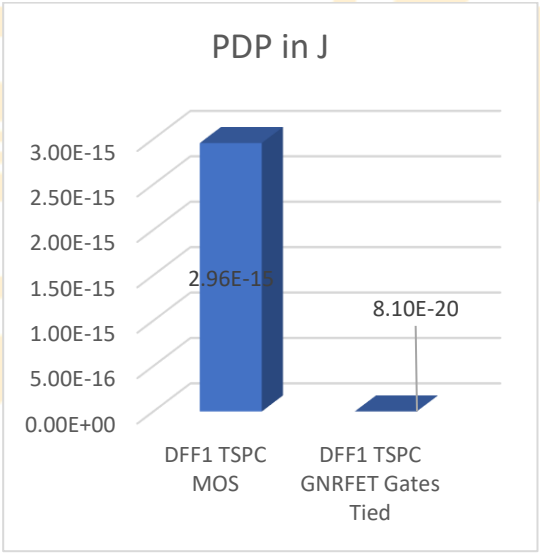

Fig. 6: PDP DFF1

Fig. 6 presents the Power-Delay Product (PDP) for the DFF1 design, demonstrating the significant improvements achieved with the TSPC GNRFET Gates Tied implementation, which outperforms the TSPC MOS design.

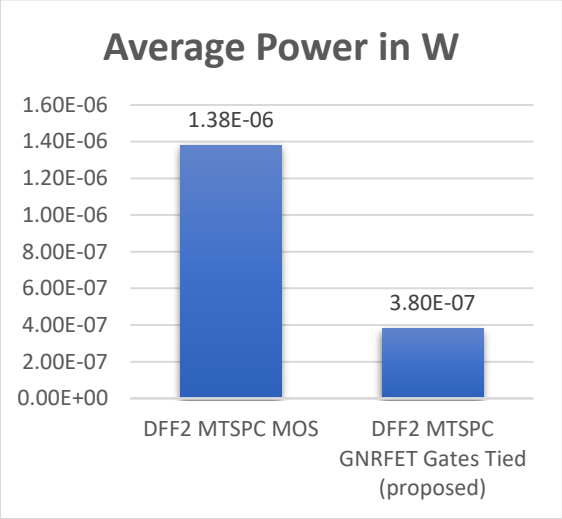

Fig. 7: Average Power DFF2

Moving on to the DFF2 design, Fig. 7 shows the average power consumption for both the MTSPC MOS and MTSPC GNRFET Gates Tied (proposed) configurations. The Gates Tied GNRFET implementation is clearly better, with lower power consumption compared to the MTSPC MOS version.

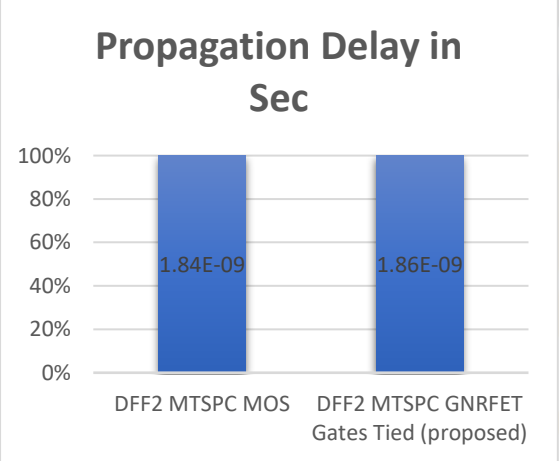

Fig. 8: Delay DFF2

Fig. 8 illustrates the delay for the DFF2 design, comparing the performance of the MTSPC MOS and the proposed MTSPC GNRFET Gates Tied implementations. Both implementations have the same delay since the circuit path between input and output is identical.

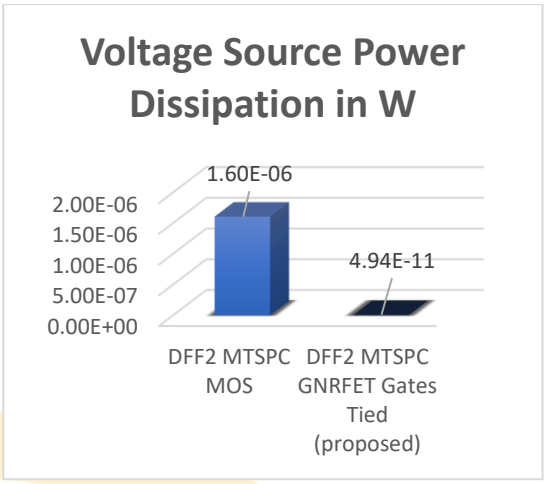

Fig. 9: Power Dissipation DFF2

In Fig. 9, the power dissipation for the DFF2 design is presented, highlighting the advantages of using the proposed MTSPC GNRFET Gates Tied approach. The Gates Tied GNRFET version exhibits significantly lower power dissipation compared to the MTSPC MOS implementation.

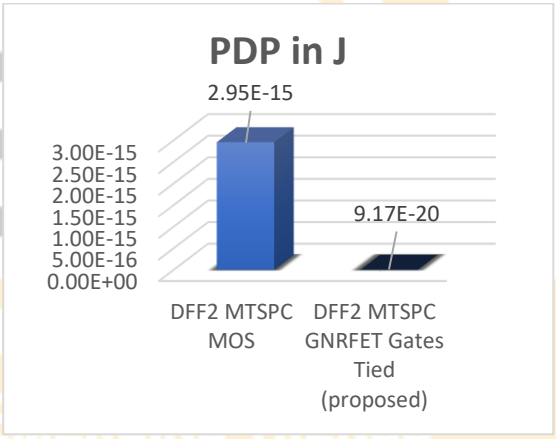

Fig. 10: PDP DFF2

Lastly, Fig. 10 demonstrates the Power-Delay Product (PDP) for the DFF2 design, emphasizing the significant improvements obtained with the proposed MTSPC GNRFET Gates Tied implementation. The Gates Tied GNRFET design outperforms the MTSPC MOS configuration in terms of PDP.

Conclusion

In conclusion, this work investigated 22-nanometer Gates Tied Graphene Nano Ribbon Field Effect Transistors (GNRFET) creation of True Single Phase Clocked (TSPC) and Modified TSPC D Flip Flops. Compared to standard MOSFET implementations, power consumption, power dissipation, and Power-Delay Product (PDP) were reduced. All configurations had the same delay since

the circuit path between input and output was the same.

Gates Tied GNRFET technology improved energy efficiency, resulting in a more environmentally friendly VLSI design. This technique might change VLSI design by offering a MOSFET option. This is crucial for low-power applications.

The discovery highlights the necessity for graphene-based electronics research, particularly given the rising need for energy-efficient and high-performance devices. More research may focus on GNRFET design and manufacturing improvements and their possible usage in additional VLSI design applications and circuits.

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