Low Power, Low EDP & High Speed based Mixed Logic 4 to 16 decoder using Shorted Gate FinFET Devices in 22nm

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ABSTRACT

Low Power optimization is one of the main factors in VLSI circuit design. In VLSI there are two type of structuring. First is Frontend and second is back end. Here in this thesis, using backend structuring. Back end designing and structuring in VLSI technology is a significant subject of research and designing as the need of low energy gadgets is sought after, it is important to make a move on circuits to diminish the energy or power utilization from at first utilized traditional circuits. Decoder is a significant circuit in the field of hardware and ICs. At first, CMOS logic is utilized for making decoder which uses 20 transistors and in blended logic same logic can be made utilizing 14 or 15 transistors however power utilization is still high. In this thesis, FinFET based blended or mixed logic line decoders for low EDP (Energy Delay Product) applications used. FinFET shows better outcomes as far as parameters, for example, Power Consumption, Delay, PDP (Power Delay Product) and EDP. 4 to 16 decoders are made utilizing MOSFET and FinFET Technology in 22nm. The decoders are proposed at based on assessment parameters and it is seen that in both design FinFET based circuits perform better than MOSFET based ordinary circuits. The last proposed circuit is made up by the use of MTCMOS, to change parameters from the existing of the last 14T or 15T based 4 to 16 decoders.
Keywords: MTCMOS, FinFET, VLSI, HSPICE, Decoder

I. Introduction:

FinFET is a promising alternative for watching out for the troubles exhibited by continued scaling. [1] Making of FinFET is acceptable with that of normal CMOS, thusly making possible exceptionally quick association to gathering. [2] FinFET devices come in various sorts. In joint or shorted gate FinFETs, the two gates are related tied, inciting a three-terminal device. This can fill in as a quick exchange for the normal mass CMOS devices. In I gate (IndependentG) FinFETs, the top bit of the gate is cut out, offering way to deal with two free gates. Since the two self-ruling gates can be controlled autonomously, IG-mode FinFETs offer more arrangement decisions. [3] Address decoder is fundamental components in all SRAM memory square which react to extremely high recurrence. [4] Access time and force utilization of recollections is to a great extent controlled by decoder plan. Structure of an irregular access memory (RAM) is commonly partitioned into two sections, the decoder, which is the hardware from the location contribution to the word line, and the sense and segment circuits, which incorporates the bit line to the information input/yield circuits. [5] Because of huge measure of capacity cells in recollections it tends to be discovered different arrangements of address decoder plans prompting power utilization decrease and execution improvement. [6]

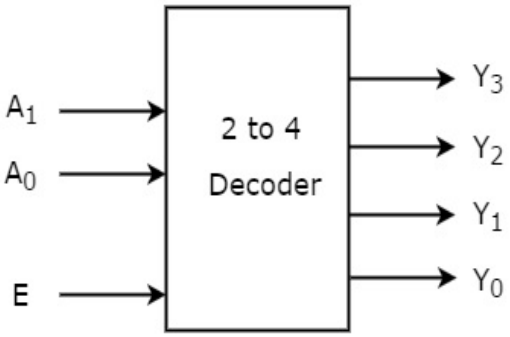

Figure 1: Symbol of decoder

The FinFET contraption includes a slim silicon body, the thickness of which is implied by TSi, wrapped by gate anodes. The present streams corresponding to the wafer plane, while the channel is confined inverse to the plane of the wafer. In light of this explanation, the device is named semi planar. [7] The free control of the front and back gates of the FinFET is practiced by drawing without end the gate cathode at the most elevated purpose of the channel. The incredible gate width of a FinFET is 2nh, where n is the amount of cutting edges and h is the parity stature. [8] Thusly, progressively broad transistors with higher on-streams are gained by using various adjusts. The sharp edge pitch (p) is the base pitch between connecting adjusts allowed by lithography at a particular innovation centre point. [9] Using spacer lithography, p can be made as half of the lithography pitch. In Digital Electronics, discrete amounts of data are spoken to by parallel codes. A parallel code of n bits is fit for speaking to up to 2^n unmistakable components of coded data. The name "Decoder" signifies to interpret or translate coded data from one arrangement into another, so an advanced decoder changes a lot of computerized input signals into a proportional decimal code at its yield. [10] A decoder is a basic circuit which takes input n and 2^n one of a kind yield lines. [11] A proficient blended rationale structure for decoder circuits, joining 32nm MOSFET, FinFET and static type CMOS. By utilizing this approach, grew new 2-4-line decoder topologies, which offer diminished transistor tally (along these lines conceivably littler format region) and improved force postpone execution corresponding to customary CMOS decoders. The device utilized will be Synopsys HSPICE which through coding in SPICE speaks to circuits and computes parameters like force, delay, and so on. The instrument for waveform review will be Avanwaves.

II. Implementation:

In 4 to 16 decoders with mixed logic, 14 T and 15T configurations are used with NAND gate for inverting type decoders. The proposed circuit is 15T based 4 to 16 decoder with MTCMOS technique added to ground terminal to improve its power configurations. The results are simulated on HSPICE under 22nm technology for FinFET channel length for decoders.

In figure 2 and 3, the block diagram of 4 to 16-bit decoder is shown in inverting mode. This requires 16 NAND gates and two 14T 2 to 4 decoder with mixed logic.

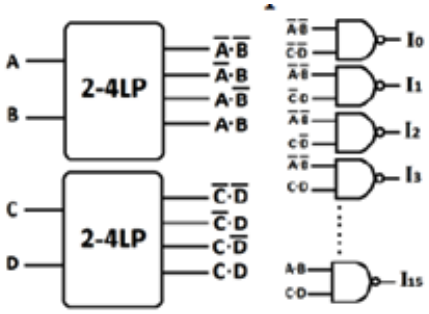

Figure 2: 14T based 4 to 16 inverting decoder block diagram

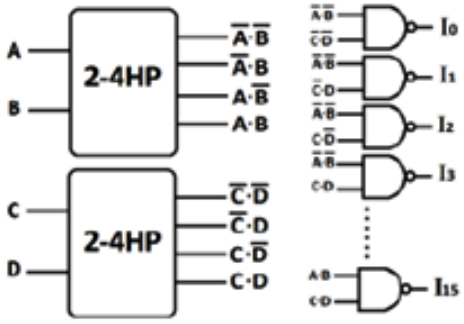

Figure 3: 15T based 4 to 16 inverting decoder block diagram

Both figure 2 and 3 circuits consist of 14T and 15T based circuits. And also 16 NAND gates and are inverting mode. These two are circuits under consideration for this thesis.
In figure 4, the final proposed circuit topology based on FinFET based MTCMOS Decoder on 4 to 16-bit configuration is presented. The Vt signal varies the threshold of the circuit. Thereby, giving chance to improve all the parameters under consideration from the ground leakage path.

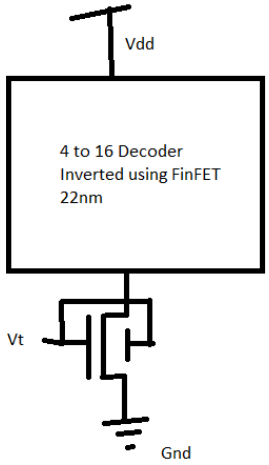

Figure 4: FinFET based 15T decoder logic 22nm with MTCMOS Signal (Proposed)

In the proposed circuit, a n type FinFET in 22nm is added as shown in figure 4 for MTCMOS benefit for power and delay and its variants.

III. Results:

The simulation results are shown in this section: in table 1, the simulation results are presented in tabular form.

Table 1: Proposed work for 4 to 16 decoders using MTCMOS based outputs

22nm	Decoder 4 to 16 with 14T MOS	Decoder 4 to 16 with 14T FinFET	Decoder 4 to 16 with 15T MOS	Decoder 4 to 16 with 15T FinFET	Proposed 4 to 16 with MTCMOS

Power Consumption	1.13E-06	3.44E-08	1.16E-06	3.91E-08	2.70E-08
Delay	7.83E-08	7.81E-08	7.83E-08	7.81E-08	7.83E-08
PDP	8.82E-14	2.69E-15	9.11E-14	3.05E-15	2.11E-15
EDP	6.91E-21	2.10E-22	7.13E-21	2.39E-22	1.66E-22

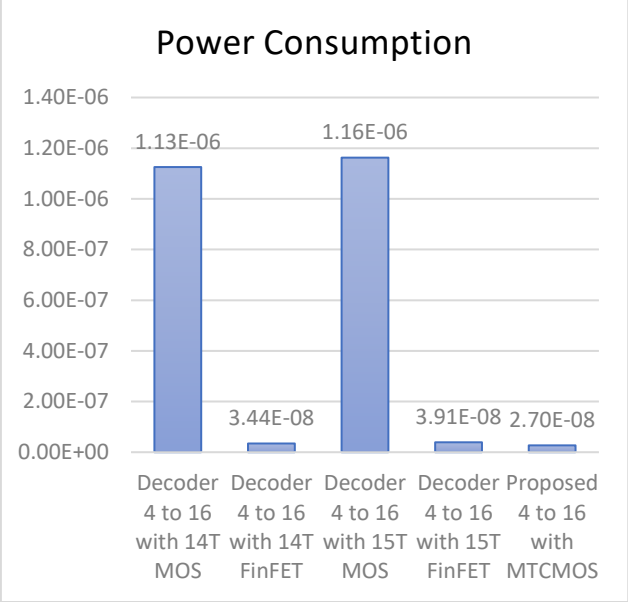

Figure 5: Outputs for Power Consumption in watt

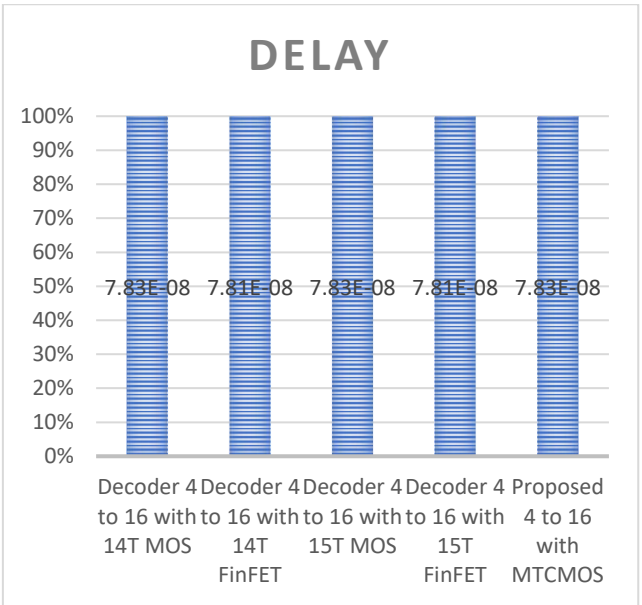

Figure 6: Outputs for Delay in sec

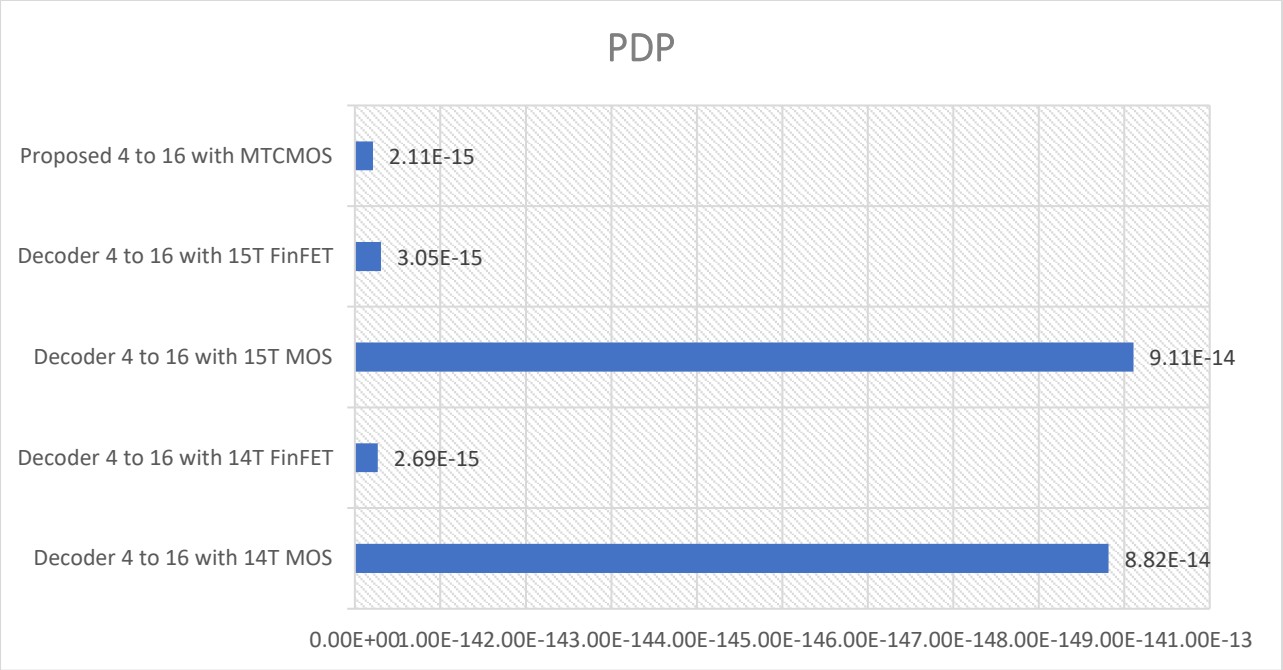

Figure 7: Outputs for PDP in Joules

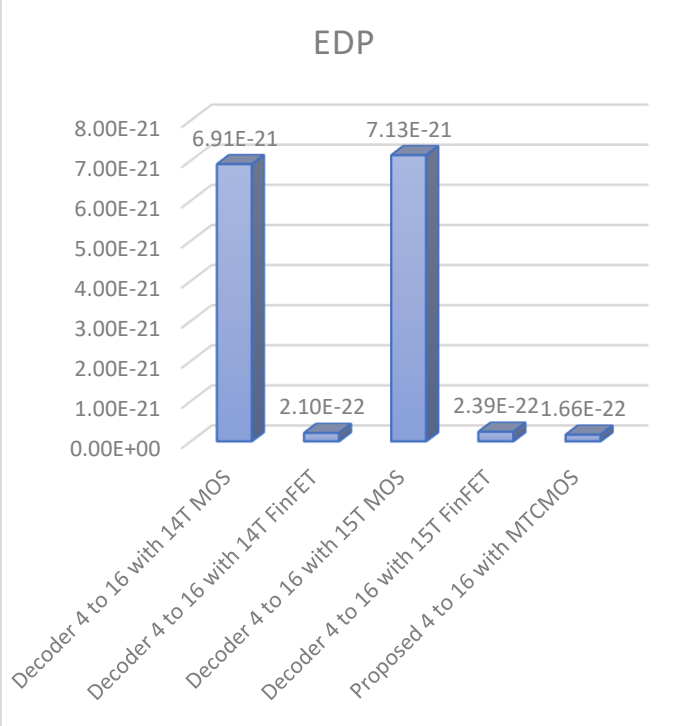

Figure 8: Outputs for EDP in Joules-sec

Figure 5 to figure 8 shows that the proposed FinFET based 22nm 4 to 16 decoder in MTCMOS mode is performing better in power consumption, PDP and EDP in all cases for 22nm technology FinFET. Delay is almost same acceptable in all cases.

IV. Conclusion:

Hence, the results were successfully implemented on Simulation platform. The following conclusions are obtained.

- The use of FinFET over MOSFET in the proposed technique reduces Power consumption; it indicated that FinFET is a promising substitute for MOSFET beyond 22nm technology.
- The reduced short channel effects in FinFET and better control over the gate of the FinFET improves the Power in designed techniques. About 90% improvement from MOSFET based circuits, high speed and low PDP and Low EDP.
- 0.02% variation in delay, all delays almost same.
- 48% improvement in power.
- 30.8% improvement in PDP and EDP.

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