ISSN: 2545-4523 (Online)

Optimizing Noise and Power of Low Pass Filter using Ring Oscillator

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Abstract— Filters are important building blocks in many analog signal processing systems. Traditional filter implementation involves the applications of two commonly used analog integrators, the Gm-C integrator and the Opamp-RC integrator. The DC gain of the two conventional analog integrators are greatly limited by the gain of operational amplifier (Opamp) used in Opamp-RC integrator or operational trans conductance amplifier (OTA) used in Gm-C integrator. Process scaling of technology available for integrated circuits is beneficial for smaller area and higher density of integrated circuits but also reduces the output impedance of the transistors, therefore further exacerbating the performance of Opamp and OTA.

This paper features applying ring oscillator integrators (ROIs) in the design of analog. ROIs implemented using simple CMOS inverters can achieve infinite DC gain at low supply voltage independent of transistor non-idealities and imperfections such as the finite output impedance. Consequently, ROI based analog filter design scales more effectively into newer technology process. The paper starts with an overview of background theory of analog filter design, followed by high order analog filter topologies constructed based on Opamp-RC integrators along with system-level behavioral simulations using HSPICE focusing on second order filters. In the second part, ROI based analog filter design is proposed with system-level analysis. The suggested filter topology is then verified by LT-spice for first order and second order analog filter design. In the third part, we will implement our proposed ROI analog filter at circuit-level using 180 nm models. Finally, we conclude our project with summary and evaluation of the research results and suggestions of possible future research and improvements of our paper.

Keywords— Analog filters; analog signal processing; continuous time filters; integrator; ring oscillator; ring oscillator integrator.

Introduction

This paper is an outcome of a study and an investigation on the design and simulation of a ring oscillator integrator based analog low-pass filter. In this paper we have designed and simulated the circuit prototype and also additionally worked out the noise analysis of their proposition. In this introductory part of the paper we shall be dealing with overview and the study on the basics of the domain area of the paper.

Filters and oscillators form a very important signal processing block. Simple analog filters could be implemented using passive elements of resistors, inductors, and capacitors only, but such implementation of filters are usually not favored as they suffer severely from loading effect. In other words, the behavior of the filters is not consistent as specified for different connections of load. Matching networks are usually required, but they only serve well for a

limited range of frequencies. Besides, the bulky volume of passive elements filters is not suitable for integrated circuit design. At integrate circuit level, analog filter designs involve the usage of analog integrators.

Analog integrators are key building blocks in signal processing with two most commonly used popular integrators; the Gm-C integrator and the Op-amp-RC integrator. The performance of these two types of the integrators are closely dependent on the operational trans-conductance amplifiers (OTAs) contained in the circuit, and the OTAs result into performance degradation on the filters due to the non-idealities of transistors in integrated circuit design. In view of the drawbacks of OTA-based integrators, the use of CMOS inverter-based ring oscillators to implement integrators (ROIs) with infinite DC gain independent of transistor dimensions and supply voltage is suggested [1]. The "digital" natures of the ROIs allow them to operate with low supply voltages and scale better with process than conventional OTA-based designs. The viability of the ROIs will be first analyzed and verified from system-level simulations throughout this paper.

I. System level implementation of ROI Filter

The theoretical basis for ROI is presented at the beginning of this section followed by an overview of the system-level block diagram is given to discuss about how the low pass behavior is realized using ROI . Section 1 features the analysis of a first order Low Pass Filter and a Two-Thomas bi-quad implementations. Ring oscillator built from CMOS inverters has the property of infinite DC gain, which is much preferred over op-amp. Thus, ROI is proposed to design an active analog filter. The most common way to design a CMOS ring oscillator is to use three inverters in a feedback loop, as shown in Figure 1.

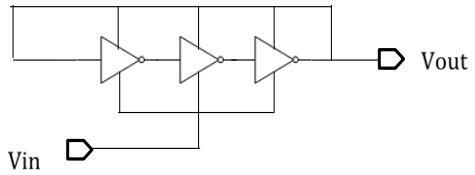

Figure 1: 3-stage inverter based voltage controlled ring oscillator

Classical techniques to increase the DC gain of the OTA include either cascoding or cascading multiple gain stages. Cascoding is generally more power efficient, but its usefulness is negated by low supply voltages in deep sub-micron processes. A multi-stage OTA can achieve both high gain and large signal swing, but requires complex compensation schemes which typically limit the integrator bandwidth. Thus, there is no clear solution to achieving high DC gain without paying a significant power or bandwidth penalty [1].

The transfer function of a 3-stage ROI reveals that a VCO acts as a true lossless integrator [2]. The PD measures the phase difference between the VCO output and the reference clock in the form of a pulse width modulated output signal. Our coming chapters illustrates the phase detector operation for two phase error conditions. Assuming the phase detector operates on only rising edges, when the rising edges of the two clocks are radians out of phase, the rising and falling edges of the output are also radians apart and the PWM output signal, D_{OUT} has 50% duty cycle. When the phase error changes, the percentage of the time that the signal is high also changes.

ISSN: 2545-4523 (Online)

While the ring oscillator achieves infinite DC gain it suffers from 4 important non-idealities: (a) Spurious tones in the output spectrum caused by pulse-width modulation, (b) nonlinearity, (c) additional phase shift caused by parasitic poles, and (d) noise. Each of these issues and their mitigation techniques are discussed. These problems are solved by taking better configurations and logical circuits while implementation like taking a 32-stage ROI instead of 3-stage ROI or we used delay cells within the Ring oscillator circuits to increase delay as it reduces the total harmonic distortions (THD). We also use symmetric XOR and level shifter to give the output for VCO a full swing voltage level that can synchronize with Phase Detector and Charge Pump. Every system is described in schematic as well as comparisons are included for better understanding of our work.

To use the oscillator, gain, a phase detector is needed to convert the output phase to pulse width modulated (PWM) voltage. The way the phase detector works is illustrated in Figure 2.

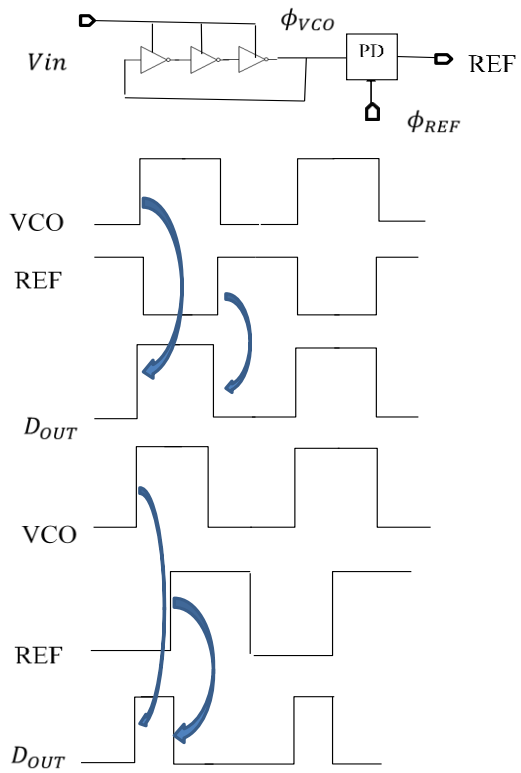

Figure 2: Phase to PWM conversion using phase detector [1].

The transfer function of the phase detector can be written as

$$H_{PD}(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = K_{PD} \qquad (1)$$

The phase detector gain K_{PD} is a constant and unit less, depending on which type of phase detector it is. For the simplest XOR phase detector, the gain is equal to$\frac{2}{\pi}$. In this design, the two-state phase detector is used and its gain is equal to$\frac{1}{\pi}$. This will be discussed later in more

detail [23, 52]. Finally a charge pump is cascaded after the phase detector to convert the PWM voltage signal to PWM current. The gain of the charge pump is simply equal to the current that the charge pump provides. That is,

$$H_{CP} = K_{CP} = I_{CP} \qquad (2)$$

Having each part of the integrator, the whole integrator schematic is shown in figure and the transfer function can be written as

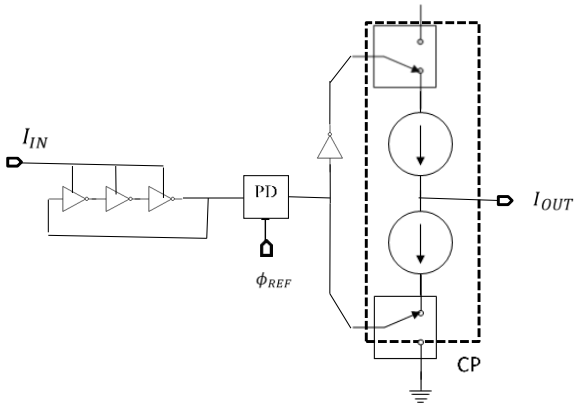

Figure 3: Ring oscillator integrator system-level schematic [4]

$$H_{INT}(s) = \frac{K_{CCO}K_{PD}K_{CP}}{s} \qquad (3)$$

Where K_{CCO} denotes current controlled oscillator gain instead of voltage controlled oscillator. The reason to work with current is that the oscillation frequency is mainly decided by the current through the oscillator. Although the input is still voltage, there is a simple way to convert the input voltage into current [13]. The biasing point of the VCO could be viewed as an AC ground, and therefore a simple resistor could perform the conversion, as illustrated in figure 4.

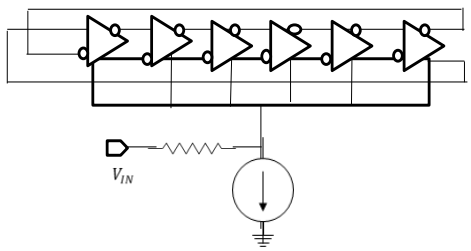

Figure 4: Input voltage-to-current conversion [4]

$$I_{in} = \frac{V_{in}}{R} \qquad (4)$$

The overall system-level schematic is shown in figure 5.

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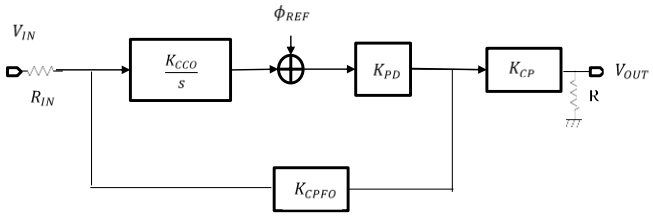

Figure 5: System-level schematic of ROI filter

The transfer function is therefore

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{R_{in}K_{CP}} \frac{1}{1+\frac{s}{K_{CCO}K_{CP}K_{PD}}} \qquad (5)$$

and the bandwidth is $K_{CCO}K_{CP}K_{PD}$.

Now, we are going to discuss the sub-circuits of the design which all combines and form an integrator. But first we have to understand the functioning of each of the circuit to bring forward an overview, how the process is going to occur.

Delay cell

Delay cell is the key component of the oscillator. Since the standard CMOS inverter only has one input/output and two differential inputs/outputs are needed. A new topology should be used to achieve this. As shown in the figure 6, the differential delay cell is composed of two inverters and two feed-forward transmission gate logics that act as two resistors.

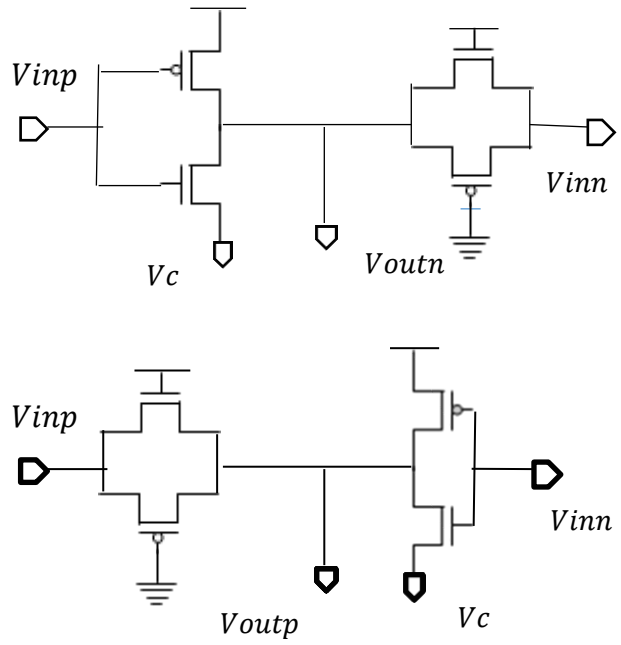

Figure 6 Differential Delay cell schematic

The constraints is that the feed-forward paths should be large enough such that the oscillator does not latch up [5]. Since the effective resistance of the transmission gate largely depends on the W/L ratio instead of the output voltage, thus R_{on} can be adjusted by varying the W/L ratio of the transmission gate to ensure that latch up does not occur.

II. Multi-phase differential ring oscillator

In this design, 12 stages of delay cells and 24 phases are used. The circuit schematic is shown in figure 7.

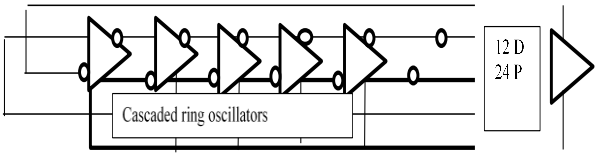

Figure 7: 12-stage ring oscillator

We have analyzed a multi-phase ring oscillator. The coupling capacitors at the output of each stage are used to add delay such that the oscillation frequency is of interest and therefore the K_{CCO}. A simple oscillator produces a periodic output, usually in form ofvoltage. As such, the circuit has no input while sustaining the output indefinitely. If the amplifier itself experience so much phase shift at high frequencies that the overall feedback become positive, then oscillation may occur [16]-[18].

Level shifters

Level shifters alter the level of a signal. It means that the level shifter circuits are used to change the level of the signal. There has been a lot of work done to reduce the power consumption of different circuits. In order to reduce power consumption while limiting the sacrifice of speed, several voltage domains may be implemented on the same IC [14].

As shown in Figure, the current controlled ring oscillator requires a current source at the bottom, which also requires some biasing voltage to make it operate normally. As a result, each oscillator output cannot achieve full swing and is limited by the biasing voltage of the current source [27]. Thus, a level shifter is employed to derive each oscillator output to full swing. Its schematic is shown in figure 8.

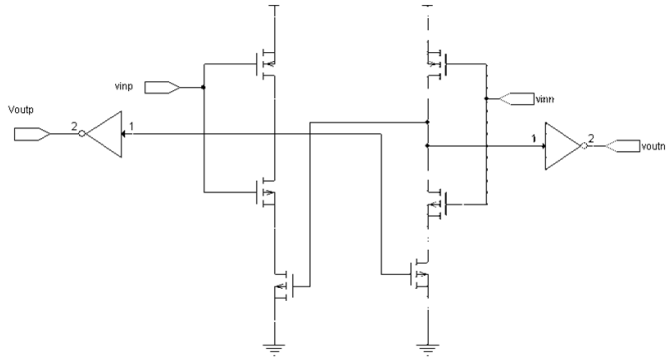

Figure 8: Level shifter

One constraint of the level shifter is that the minimum value of the input voltage should be as small as possible. In other words, the biasing voltage of the current source should be as small as possible; otherwise, the level shifter could not function normally.

III. Phase detector

The phase detector in this design is chosen to be the two-state phase detector. The schematic is shown in figure 9.

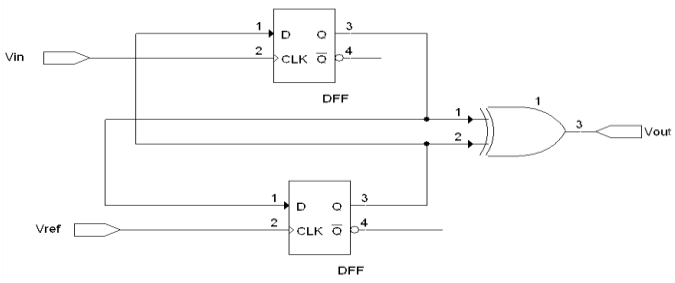

Figure 9: Two-state phase detector scheme

It is composed of two differential D flip-flops and an XOR gate. The phase detector input is connected to the CLK of D flip-flop instead of D and the circuit will settle down after a short time. The phase detector output is the same as the XOR, and the last inverter is just used to generate the complement signal. The main advantage over an XOR-only phase detector is that it has half the output frequency and gain, thereby reducing the power dissipation in switching charge pumps [3].

Differential D flip-flop

Since differential signals are applied in this filter, the D flip-flop of the phase detector also should support such characteristics. A good example is illustrated in [5] and the schematic is shown in figure [10].

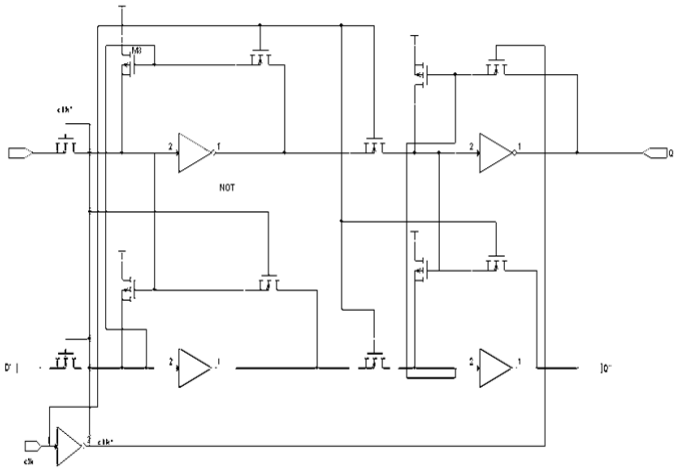

Figure 10: Differential D flip-flop schematic [5]

This kind of differential D flip-flop exhibits less power and moderate delay compared with a sense amplifier flip-flop and static single-transistor clocked flip-flop [5]. It also requires both the CLK signal and its complement, which is more favorable for this phase detector since the

input is connected to the CLK port instead of D. For other applications where exact timing is needed and the complement of CLK is not preferred, this differential D flip-flop might not be favorable.

Symmetric XOR

There are several possible schematics for the XOR gate as shown in figure 11 that require only six transistors. However, the problem is that complementary inputs are not available. Also, the delay time for different input patterns will vary largely.

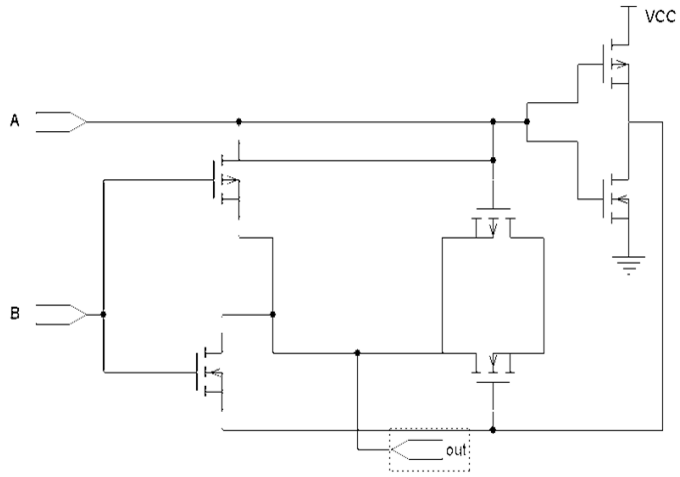

Figure 11: Sample XOR gate schematics with fewer transistors [13]

To remedy these effects, a symmetric XOR is proposed as shown in figure 12.

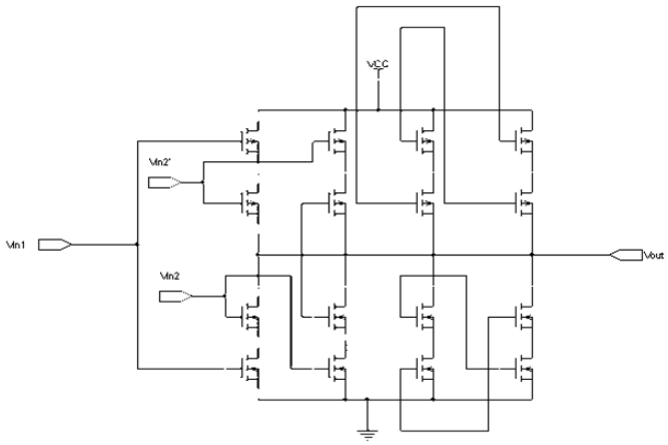

Figure 12: Symmetric XOR gate schematic [11]

It has both two input signals and their complements. In addition, the right side, which is the dual of the left side, ensures that the delay is the same for all input patterns.

IV. Charge pump

The charge pump, shown in figure, converts the PWM voltage signal into PWM current.

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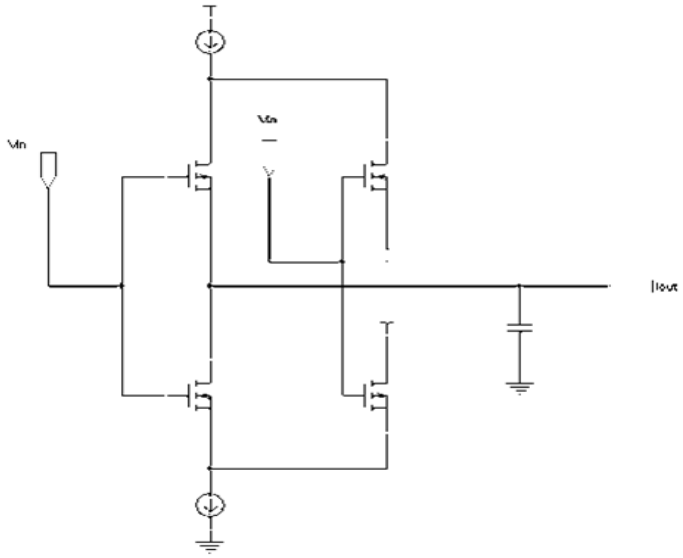

Figure 13: Charge pump schematic

When input is high, the two PMOS are off and the two NMOS are on, which makes the bottom current source connected to the output. This will force more current through the CCO. On the contrary, when input is low, the two PMOS are on and the two NMOS are off, which makes the top current source connected to the output. This will draw the same amount of current from the CCO [12].

V. Output stage

The output stage for each stage is composed of an inverter and a resistor as shown in figure. All phase outputs are connected in parallel.

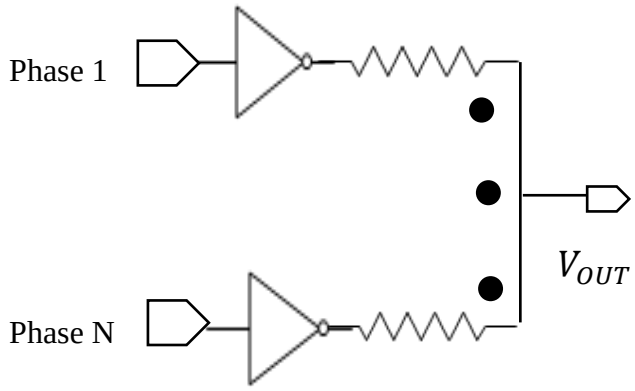

Figure 14: Output stage

The filter bandwidth can be tuned most conveniently by varying the feedback charge pump current and thus changing. Because the charge pump non-linearity is independent of its current, tuning does not degrade distortion performance of the filter. This is in contrast to conventional filter tuning schemes which often require a non-linear tuning element, such as the MOSFET in R-MOSFET-C filter [17]. Having presented the implementation of a first order low pass filter, the next section describes the design details of a fourth order Butterworth low pass filter implemented in the prototype IC. Chapter 4 starts discussion about the implementation of LPF with ROI as the key component.

Design and Simulation results of ROI Filter

ISSN: 2545-4523 (Online)

In this section, the design of the constraints are discussed. We include gain of Current controlled oscillator, gain of Phase Detector and input resistance *Rin* and some issues related to these parameters.

Simulation result

Analysis of Level shifter

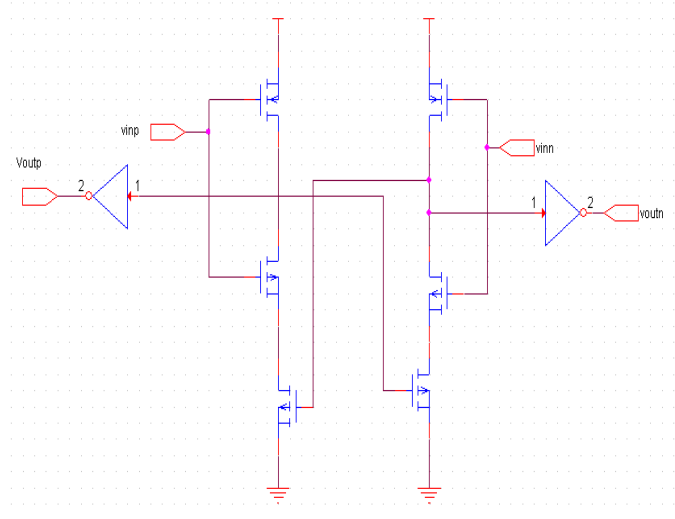

Figure 15: Schematic for level shifter

Above figure shows a schematic for level shifter. In the figure If Vin- is small enough, only PMOS will be on. This will turn on the bottom NMOS, which in turn pulls the input of Vout + to ground. However, when Vin+ is Vdd and Vin- just exceeds the threshold voltage of NMOS, both the top NMOS and PMOS on the right branch will be on. Since the top NMOS at the right branch, and eventually the left intermediate node will reach ground..

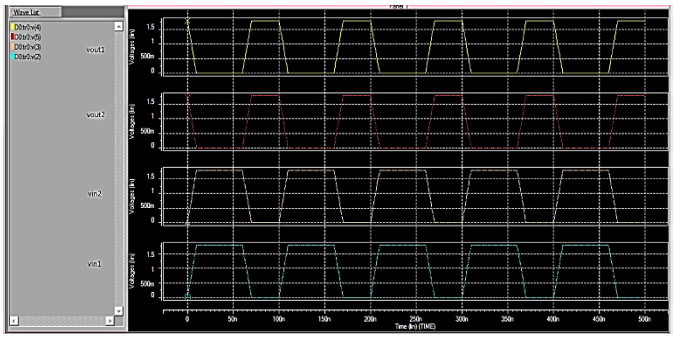

Figure 16: Output for level shifter

Analysis of D Flip-Flop

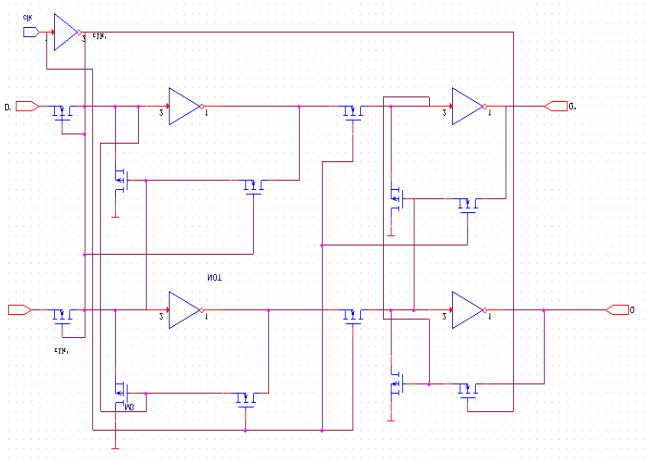

Figure 17: Schematic for D Flip-Flop

This kind of differential D flip-flop exhibits less power and moderate delay compared with a sense amplifier flip-flop and static single-transistor clocked flip-flop [5]. It also requires both the CLK signal and its complement, which is more favorable for this phase detector since the input is connected to the CLK port instead of D. For other applications where exact timing is needed and the complement of CLK is not preferred, this differential D flip-flop might not be favorable.

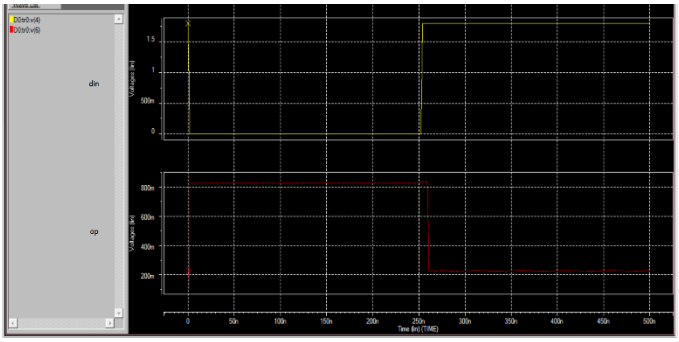

Figure 18: Output for D Flip flop

Analysis of Symmetric Xor

The outputs of the XOR/XNOR gate are the PWM signals generated by the PD. INC represents “increment” which indicates that the frequency of the oscillator is increased over the reference frequency, while DEC represents “decrement” which indicates that the frequency of the oscillator is decreased below the reference frequency.

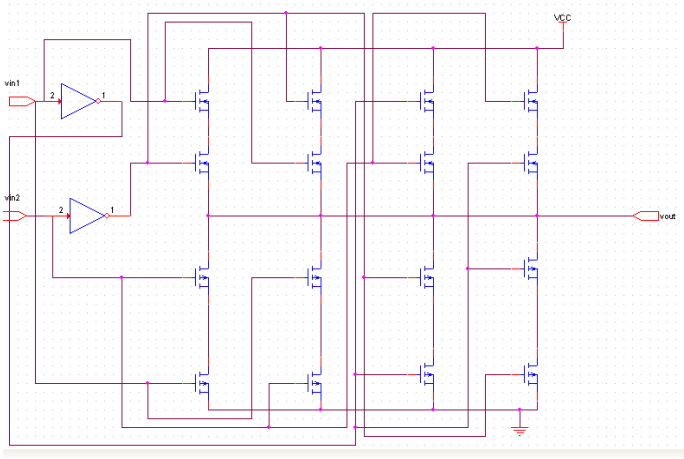

Figure 19: Schematic for Symmetric Xor

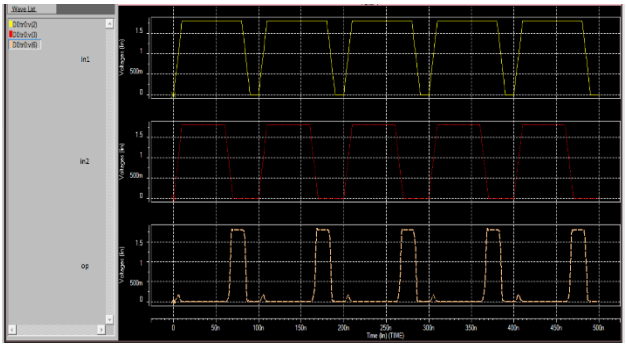

Figure 20: Output for symmetric Xor

Analysis of Ring oscillator

The circuit comprises of 12 ring oscillator cells cascaded together to give a 24 phase output with constraints like capacitance and feedback. It can be connected further to the later implemented circuits.

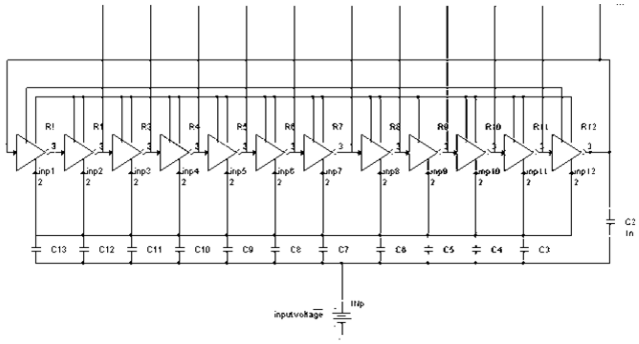

Figure 21: Schematic for 12-stage 24 phase ring oscillator [1]

We have analyzed a multi-phase ring oscillator. The coupling capacitors at the output of each stage are used to add delay such that the oscillation frequency is of interest and therefore theK_{CCO}. A simple oscillator produces a periodic output, usually in for of voltage. As such, the circuit has no input while sustaining the output indefinitely. If the amplifier itself experience

so much phase shift at high frequencies that the overall feedback become positive, then oscillation occur.

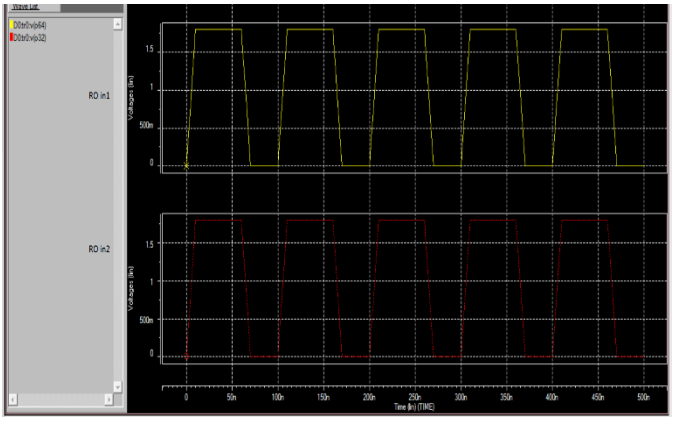

Figure 22: Output for 12 stage ring oscillator (single cell)

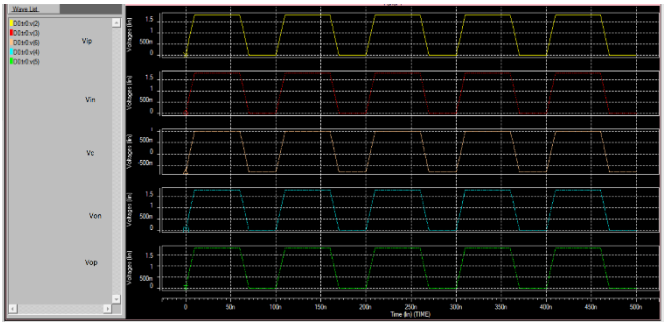

Figure 23: Output for 12 stage ring oscillator (32 cells)

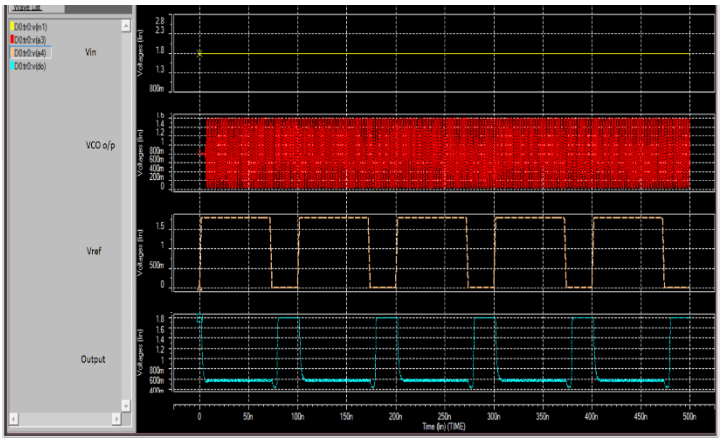

Figure 24: Output for 3 stage Ring oscillator

The result is simulated by applying different voltage sources, running transient analysis, to figure out the gain at each input frequency, and connecting them together. Figure shows the procedure in p-spice. The upper two plots are the time domain input and output signal. From the figure 24, it is clear that the oscillation frequency has been pushed to N times higher (N*120MHz=1.44GHz).

VI. Noise analysis and Power analysis

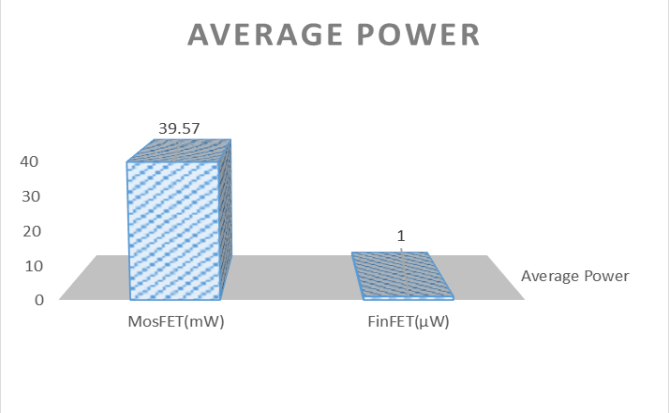

Figure 25: Average power analysis

Output Noise Average

Table 4.2: Noise and power analysis

MosFET	Fin FET
$822(\mu V)$	$2.17(\mu V)$
39.57mW	$1\mu W$

All the work done previously assumes that the perfect and free of noise. However, in the real environment is world, there are different kind of noise that could degrade the circuit performance. In this design, the noise comes from all three parts of the integrator: CCO, Phase detector, and charge pump. In, the input-referred noise is summarized to be

$$S_i = S_{\phi,CCO}\left(\frac{s}{K_{CCO}}\right)^2 + S_{PD}\left(\frac{s}{K_{CP}K_{CCO}}\right)^2 + S_{i,CP}\left(\frac{s}{K_{CCO}K_{CP}K_{PD}}\right)^2 \quad (6)$$

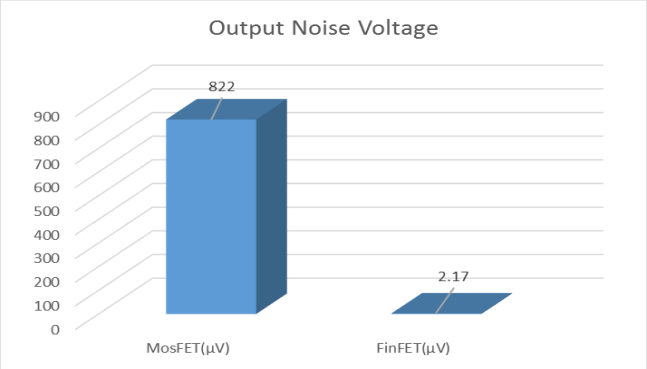

Figure 26: Output Noise Voltage analysis

Nevertheless, due to the constraint of EWS itself (insufficient disk memory), the matrix that captures noise, SNR, could not be well simulated [16, 17]. It can be simulated using high configuration disks and processors with faster clock cycles.

Conclusion

The filter exhibits reasonable and expected behavior. Ring oscillator integrators (ROIs) present time-based means to implementing analog signal processing functions. With ROI, we come to know some additional structures that are helpful in some complicated signal processing and solving them easily. By analyzing many different configuration for same circuit we come to know each pros and cons of them. In contrast to conventional voltage, current, or charge based integrators that require high gain operational trans-conductance amplifiers, ROIs implemented with simple CMOS inverters achieve infinite DC gain even at low supply voltages and independent of transistor non-idealities and imperfections such as finite output impedance. Consequently, ROIs scale more effectively into newer processes. A prototype filter with 32 delay cells designed using the ROIs was fabricated in a 180nm CMOS process to validate the proposed techniques. While operating at a supply voltage of 0.55 V, the prototype filter achieved state-of-the-art noise and linearity performance.

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